COTS JOURNAL

Tech Focus: 1553 Boards Roundup

LARGE UAV PAYLOADS

SPIRAL TOWARD AUTONOMY

PLUS:

ATCA Finds Mindshare in Military System Designs

GPPs, DSPs and FPGAs Jockey for Signal Processing Dominance

Volume 10 Number 04 April 2008 www.cotsjournalonline.com

An RTC Group Publication

Open Modular Solutions for Defense and Aerospace

OPEN

To Exceed Your Demands

➤ **AM4100**

➤ **CP6001-R2**

➤ **AT8030**

➤ **PowerEngine7**

No matter what the arena, up-to-date information is critical for successful operations. Performance and reliability go hand in hand. That's why Kontron is dedicated to bringing you the latest in AdvancedTCA, MicroTCA, VME and CompactPCI solutions and services for Defense and Aerospace. We offer exactly what you need, not only exceptional products, but a partner who will work with you from start to finish.

Whether you're designing for the battlefield or the office, we have the right solution for you.

www.kontron.com

CompactPCI® AdvancedTCA™ VMEbus µTCA™ AdvancedMC™ intel Embedded and Communications Alliance

kontron

1-888-294-4558 - info@us.kontron.com — EMEA: +49 0 800 7253756 - Asia: +886 2 2910 3532

COTS JOURNAL

Features

April 2008 Volume 10 Number 4

Departments

Coming in May...
...See Page 60

Special Feature

Large UAV Payload Challenges

Tech Recon

ATCA-Based Military Systems

System Development

GPP, DSP, FPGA Trade-Offs

Technology Focus

1553 Boards

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

Cover Story Page12

Northrop Grumman plans to incorporate radar onto the MQ-8B Fire Scout UAV. A demonstrator carrying both radar and an electro-optical/infrared system is planned for the MQ-8B Fire Scout this year on a company-owned Fire Scout using a Telephonics RDR-1700B maritime surveillance and imaging radar. Shown here, Northrop Grumman's RQ-8 Fire Scout UAV successfully test fires one of its two Mark 66 unguided rockets during weapons testing at Arizona's Yuma Proving Grounds in July of 2005.

Courtesy: Northrop Grumman

Innovation sets us apart

Avionics Databus Test, Simulation & Embedded Solutions

Lightweight, small, rugged, reliable, feature rich and cost-effective. These are only a few of the benefits of the new AB2000 series of Avionics BusBoxes® from Ballard Technology. They deliver outstanding avionics performance with multi-protocol and flexible expansion capabilities. Conductively cooled, the AB2000 is ideal for rugged avionics applications such as serving and recording data, converting protocols and providing federated control. Find out today how AB2000 innovation can work for you.

The AB2000 offers multi-protocols in a single, light-weight rugged format.

ARINC 429
MIL-STD-1553
Ethernet
RS232/422
Digital I/O
USB

Innovation for your success

For more information call 425.339.0281 or visit us at www.ballardtech.com

Ballard TECHNOLOGY

Publisher's Notebook

One Small Step, One GIANT LEAP

COTS Journal hailed as being ahead of its time once again… well almost. Ten years ago when we started *COTS Journal* we were told that we were crazy. There were only a handful of "commercial" suppliers seriously interested in delivering embedded electronics to the military, and some of those wanted to reduce their commitment in favor of the telecommunications market. Today the embedded military market segment is one of the shining stars in the merchant computer market, and we continue to be the book of record covering the technology for this market.

Here's how the "well almost" came about. COTS electronics and software in space versus the military is a little like relating performance racing to the automotive industry. To date we have COTS products in space and on Mars, and over time COTS will have more and more market penetration there. In comparison to the military market, space is a very small market, but it's growing. Couple the small market size of space systems with its extreme reliability requirements—more extreme even than most military systems—and it's clear that this market area isn't destined to be the next dot-com explosion. As we did when we were envisioning *COTS Journal*, we "embedded" our potential editorial team into the market to develop not only a market understanding, but also a relationship with all the different elements of that market.

Many military systems do operate in space or in near space environments, but those applications tend to be very open to editors prying and writing about technical issues. For the last year or so our editorial team has been "embedding" itself into elements of the non-military space technology community. Until recently our editorial participation at such events as the Space Shuttle launches has been as outsiders looking in. After all, most of the editors covering space technology have been doing so for decades, and we've only been attending for a little over a year. Most recently, Warren Andrews, Editorial Director, and myself decided to torture our bodies by attending the STS-123 Shuttle launch. The STS-123 launch (see photo) took place at 2:28 A.M. EST—I repeat A.M. We didn't get back to our hotel rooms until after 5 A.M. I can't tell you how many decades, well, years ago, it was when I last did an all-nighter.

The late launch time—or early depending on if you stayed up all day or not—gave us a lot of time to talk with the other journalists in attendance and get comments and opinions that never hit print, regarding technology, suppliers and politics: all critical information regarding a market's direction and potential. In anticipation of a long night, I brought along the latest issue of a clearly visible *COTS Journal* so that Warren and I could go over it and find ways that we may improve it. Although we've had industry discussions with editors and industry representatives at previous NASA events, at this one we felt more like members of the team rather than the outsiders we used to feel like.

To our amusement, we discovered that many of our fellow journalists at the launch mistook the term COTS on our badges. We had to explain that *COTS Journal* covers the severe environment electronics market. They thought COTS meant the "Commercial Orbital Transportation Service" market—which is an emerging concept in their world. And as a result, they assumed our magazine was way ahead of its time. But then again it was 10 years ago that we came up with the crazy notion of filling the unfulfilled need of presenting and writing about technology needs of the defense industry. Maybe a spin-off called "COTS Space Journal" isn't such a crazy idea after all. I could almost see it in my then sleep-deprived state:
One small step for Journalism, one giant leap for COTS.

Pete Yeatman, Publisher
COTS Journal

COTS JOURNAL Defense Electronics and Computing

Publisher

PRESIDENT
John Reardon, johnr@rtcgroup.com

PUBLISHER
Pete Yeatman, mail@yeatmangroup.com

EDITORIAL DIRECTOR / Associate Publisher
Warren Andrews, warrena@rtcgroup.com

Editorial

EDITOR-IN-CHIEF
Jeff Child, jeffc@rtcgroup.com

CONTRIBUTING EDITOR
David Cotton, davidc@rtcgroup.com

MANAGING EDITOR
Marina Tringali, marinat@rtcgroup.com

COPY EDITOR
Rochelle Cohn

Art/Production

CREATIVE DIRECTOR
Jason Van Dorn, jasonv@rtcgroup.com

ART DIRECTOR
Kirsten Wyatt, kirstenw@rtcgroup.com

GRAPHIC DESIGNER
Christopher Saucier, chriss@rtcgroup.com

DIRECTOR OF WEB DEVELOPMENT
Marke Hallowell, markeh@rtcgroup.com

WEB DEVELOPER
Brian Hubbell, brianh@rtcgroup.com

Advertising

WESTERN REGIONAL ADVERTISING MANAGER
Stacy Gandre, stacyg@rtcgroup.com
(949) 226-2024

WESTERN REGIONAL ADVERTISING MANAGER
Lauren Hintze, laurenh@rtcgroup.com
(949) 226-2014

EASTERN REGIONAL ADVERTISING MANAGER
Nancy Vanderslice, nancyv@rtcgroup.com
(978) 443-2402

EASTERN REGIONAL ADVERTISING MANAGER
Todd Milroy, toddm@rtcgroup.com
(267) 247-5866

INSIDE SALES MANAGER
Carrie Bowers, carrieb@rtcgroup.com
(949) 226-2029

BILLING
Maggie McAuley, maggiem@rtcgroup.com
(949) 226-2024

COTS Journal

HOME OFFICE

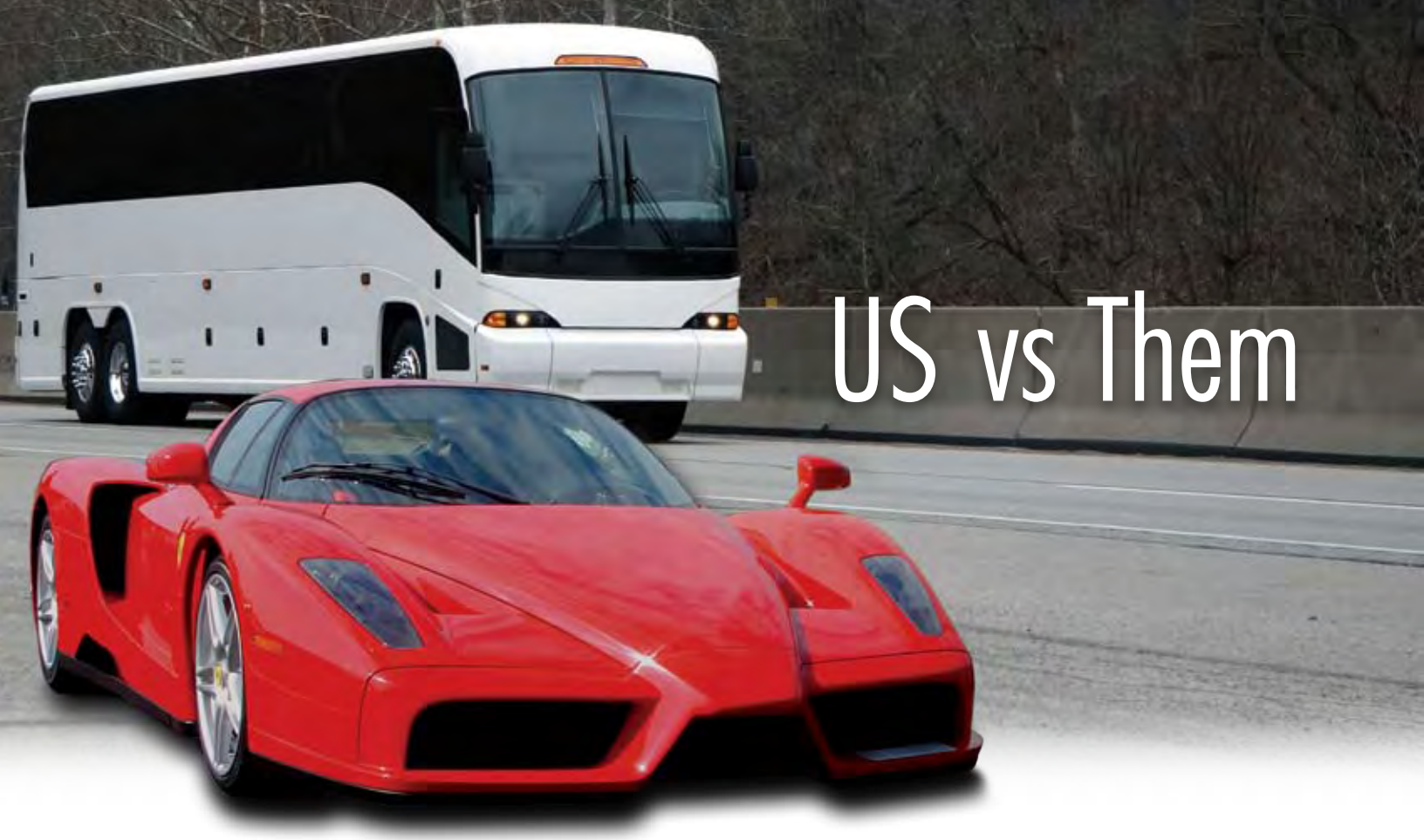
The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673
Phone: (949) 226-2000 Fax: (949) 226-2050, www.rtcgroup.com

EDITORIAL OFFICES

Warren Andrews, Editorial Director/Associate Publisher
39 Southport Cove, Bonita, FL 34134
Phone: (239) 992-4537 Fax: (239) 992-2396

Jeff Child, Editor-in-Chief
20A Northwest Blvd., PMB#137, Nashua, NH 03063
Phone: (603) 429-8301 Fax: (603) 424-8122

Published by THE RTC GROUP



US vs Them

Other than the fact that we may be in the same industry, that is where the comparison ends...

Complete Precision Engineering –Solutions that fit your every need

Our exquisite products and custom design expertise help our clients to quickly meet complex design requirements.

Our service to the aerospace and telecommunications markets has resulted in a quickly growing line of AdvancedTCA, MicroTCA, AMC, cPCIe, VXS, XMC and custom boards for processing, communication, storage, and platform interoperability.

At VadaTech we differentiate ourselves from other embedded computer manufacturing companies by incorporating our customers' vision into the product specification and development process; all the way through to deployment. Our partnership philosophy with our customers expands their engineering resources, increasing their value.

You deserve the best, let VadaTech help you become the benchmark for your industry.

VadaTech is a leader in:

- AdvancedTCA
- MicroTCA
- cPCIe
- XMC
- AMC
- VXS
- Custom Board-Level Technology

AMC220

The AMC220 is a two port 10-Gigabit Ethernet (10GbE) AdvancedMCTM (AMC) module which includes an on-board linerate multi-core packet processor. VadaTech offers this product in a mid-height form factor based on the AMC.1 specification.

vadatech inc.
THE POWER OF VISION

WWW.VADATECH.COM
TEL 1.702.896.3337

GE Fanuc
Intelligent Platforms

Your ticket to the Express bus.

Get on the Express bus with GE Fanuc Intelligent Platforms.

A flight line specialist has to have speed and mobility. The latest rugged laptops, with ExpressCard slots, have both. And we have the cards you need to take advantage of this new technology.

With a full selection of ExpressCards, GE Fanuc Intelligent Platforms covers the major avionics protocols: MIL-STD-1553, ARINC 429 and AFDX. And these cards are fast. For example, our AFDX card can capture full rate AFDX bus traffic—on a fully loaded bus.

To make the upgrade as easy as possible, we offer these new ExpressCards in several configurations; from card only, to card plus bus analyzer, to a turn-key system with the card, the laptop and the pre-loaded analyzer.

For all the details, please visit our web site, and put your avionics tools on afterburner.

www.gefanucembedded.com/avionics

MIL-STD-1553, ARINC 429 and AFDX ExpressCards available.

GE FANUC

The Inside Track

FLIR Systems Delivers First MEP Sensors for Small UAVs

FLIR Government Systems, a division of FLIR Systems, recently delivered the first of three Mission Equipment Package (MEP) sensors to the U.S. Army's Night Vision and Electronic Sensors Directorate (NVESD). The sensor has been integrated into NVESD's UH-1 test helicopter and has successfully completed its first flight providing excellent imagery and demonstrating many of the key features. Additional flights are planned throughout the spring to fully characterize the system capabilities. MEP is a reconnaissance, surveillance, target acquisition with laser designator (RSTA+LD) sensor that is now being targeted for Tier II (Figure 1) and other small unmanned aerial vehicles (UAVs). However, the small size, low weight and simple integration make MEP an ideal sensor whenever height, size and weight are at a premium. This includes a wide range of air, ground and maritime platforms.

Figure 1

MEP is a reconnaissance, surveillance, target acquisition with laser designator sensor designed for use in Tier II and other small UAVs. The Army's Shadow is an example of that class of UAV. Shown here, an Army Specialist prepares a Shadow 200 UAV for launch at Forward Operating Base Warhorse, Iraq.

The MEP features five sensors: two IR cameras, a color TV camera, a laser rangefinder and a laser designator. One key feature of the MEP is the secondary steering system (SSS). This feature provides a cooperative wide field of view (WFOV) and narrow field of view (NFOV). The WFOV IR is mounted on an internal gimbal. The WFOV IR is used to detect potential targets of interest, and the NFOV IR with its improved range performance is used to identify, track and designate the targets. Integration of the MEP is facilitated by a single connector, containing both power and an Ethernet connection. All of this is packaged in a system that is 7.25 inches in diameter and weighs less than 16 pounds. FLIR Systems intends to deliver the remaining two MEPS by the end of 2008.

FLIR Systems
Wilsonville, OR.
(800) 322-3731.
[www.gs.flir.com].

DataPath Awarded Contract for U.S. Army SATCOM Terminals

DataPath has been awarded $6.6 million to continue resets, repairs and upgrades to DataPath Satellite Transportable Terminals (STTs) and Unit Hub SATCOM Trucks (UHSTs) used in the U.S. Army's Joint Network Node (JNN)/ Warfighter Information Network-Tactical (WIN-T) program. This delivery order is part of a previously announced four-year contract with the Army that has a potential value of up to $270 million for the company. Work under the delivery order includes resets and repairs to terminals returning from the battlefield, as well as upgrades that include compatibility for Wideband Global SATCOM (WGS) Ka band and cold weather operation. DataPath engineers and field technical experts will perform the work at DataPath's facilities as well as at various Army locations. The Program Manager for WIN-T's Commercial SATCOM Terminal Program at the U.S. Army Communications-Electronics Command in Fort Monmouth, N.J., awarded the delivery order through the Worldwide Satellite Systems contract.

DataPath
Duluth, GA.
(678) 597-0300.
[www.datapath.com].

Quintron Provides Mission Voice System for ULA Rocket Launch

Quintron Systems participated in the successful launch of the first United Launch Alliance (ULA) Atlas V rocket from Space Launch Complex 3 (SLC-3) at Vandenberg Air Force Base (VAFB) on March 13th (Figure 2). Quintron provided a DICES mission voice system to the previous Atlas launch operations from SLC-3 in 1997, comprised of two physical switches. One was installed for launch pad operations with a second for the Remote Launch Control Center (RLCC) located approximately 16 miles from SLC-3.

Following the selection of DICES for Atlas V launch support from Cape Canaveral in 2000, Lockheed Martin took over the earlier DICES equipment still in place at SLC-3 from Atlas 3 operational period as the baseline for upcoming Atlas V launches from VAFB. Starting in 2004, significant upgrades and enhancements were introduced to both the SLC-3 and RLCC DICES systems, including a completely new communications package on the launch

Figure 2

An Atlas V rocket launches on March 13 from Vandenberg Air Force Base with the aid of Quintron Systems' DICES device.

tower itself. This was required to provide improvements needed for hazardous operations inherent in the Atlas V rocket. The Atlas V is the latest in a family of launch vehicles stretching back fifty years, providing support for American defense and space exploration missions in numerous programs. The payload for this first VAFB Atlas V launch was a National Reconnaissance Office satellite.

Quintron Systems
Santa Maria, CA.
(805) 928-4343.
[www.quintron.com].

Retired 4-Star General Peter Pace to Chair Board for Pelican

Pelican Products, a manufacturer of advanced lighting systems and rugged cases, has appointed retired Marine Corps General Peter Pace (Figure 3) as its Chairman of the Board. Pace is the former Chairman of the Joint Chiefs of Staff and a four-star general. Pace assumes the Chairman of the Board position at Pelican in a non-executive role and will provide additional strategic oversight to Pelican's work in the military, defense and federal government sectors. He succeeds Rob Gluskin, a Behrman Capital operating partner, who will continue to serve Pelican as director. Pelican Products is known for developing the high-quality, military-grade protector cases, flashlights and lighting systems in the world.

Figure 3
Retired Marine Corps Four-Star General Peter Pace served as the 16th Chairman of the Joint Chiefs of Staff from September 2005 to October 2007. He is the first Marine to have served as Chairman of the Joint Chiefs of Staff.

Pace, 62, served as the 16th Chairman of the Joint Chiefs of Staff, the most senior position in the United States Armed Forces, from September 2005 to October 2007. In his capacity as Chairman, he served as advisor to the President, Secretary of Defense, the National Security Council and the Homeland Security Council. Pace served as the Vice Chairman from 2001 to 2005. He is the first Marine to have served as either Chairman or Vice Chairman of the Joint Chiefs of Staff.

Pelican Products
Torrance, CA.
(310) 326-4700.
[www.pelican.com].

Expand Networks Secures Army WIN-T Optimization Contract

General Dynamics C4 Systems (GDC4S) and the U.S. Army has awarded the Warfighter Information Network – Tactical (WIN-T) Increment 2–3 TCP Performance Enhancing Proxy (PEP) contract to Expand Networks. Expand Networks is porting the Accelerator Operating System to General Dynamics' WIN-T hardware platform. The Expand PEP will operate in a mobile ad-hoc environment where dynamic outbound links are created and broken frequently, providing warfighters with maximum communications efficiency on the move as well as at the halt.

WIN-T is the U.S. Army's on-the-move, high-speed, high-capacity backbone communications network, which links ground-level warfighters with commanders and the DoD's Global Information Grid. Expand's complete WAN Optimization solution will be available on the WIN-T blade to increase throughput, accelerate application performance and interoperate with other communications nodes equipped with Space Communications Protocol Standard (SCPS- TP) Acceleration devices. The Expand PEP mitigates the effects of latency and ensures that tactical networks deliver maximum performance. More than 9,000 Expand Accelerators have been deployed in networks throughout the U.S. government and in all branches of the Military.

Expand Networks
Roseland, NJ.
(973) 618-9000.
[www.expand.com].

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

LDRA's Tool Suite Selected for Orion CEV Space Program

Lockheed Martin has selected the LDRA tool suite to enable developers on the Orion Crew Exploration Vehicle (CEV) program to achieve its software development goals. Aimed at safely transferring astronauts to and from the International Space Station (ISS), the Moon, Mars and other destinations beyond low earth orbit (LEO), the Orion CEV is a state-of-the-art human space flight system. LDRA, the leading provider of automated software verification, will enable Orion developers to achieve the stringent safety-critical standards required to ensure safe transfer of the astronauts.

NASA has awarded Lockheed and its subcontractors a multimillion-dollar contract for Orion's development. Orion CEV will replace the space shuttle scheduled to be retired in 2010. Its first manned mission is targeted for 2014. LDRA's Testbed and TBrun tools have been selected to assist in the Orion project. LDRA Testbed, the process management tool at the core of the LDRA tool suite, forms the foundation of automated software verification. LDRA Testbed performs the code, quality and design reviews on the source code. It conducts test verification for code coverage, including statement, branch/decision, test path (LCSAJ), procedure/function call metrics and provides access to the Test Manager. TBrun, LDRA's automated unit testing tool, has taken a significant step further than other vendors. With TBrun, a GUI interface automates the production of test data vectors with test harness and stub generation completing automatically.

Figure 4
NASA's Orion Crew Exploration Vehicle (CEV) will replace the space shuttle scheduled to be retired in 2010. Its first manned mission is targeted for 2014. This artist's rendering represents a cut-away concept of the Orion Crew Exploration Vehicle's crew module.

LDRA
Monks Ferry
Wirral, UK.
+0151 649 9300.
[www.ldra.com].

COTS Websites

www.usdc.org

USDC Website Is Grand Central for Display Technology

The US Display Consortium (USDC) is an industry-led public/private partnership providing a common forum for flat panel display manufacturers and developers, FPD users and the supplier base. The consortium's primary mission is to manage supply-chain projects and share the results with USDC member companies. The USDC also provides a communication channel among industry, government and the financial communities for display issues.

The USDC Technical Program was initially funded by DARPA and has since been transferred to the Army Research Laboratory (ARL). Each year the ARL provides

funding to the USDC to allocate to technical projects of interest. The mission of the ARL is to enable technologies that will meet future Army combat needs and solve the critical technical barriers that limit the performance, reliability, functionality and affordability of battlefield systems. The USDC/ARL partnership funds technology advancements in the display supply chain that will meet military needs and consumer requirements to fuel further industry growth.

US Display Consortium, San Jose, CA. (408) 993-8111. [www.usdc.org].

Special Feature

Large UAV Payload Challenges

Payloads Empower Autonomy Trend for Large UAVs

Large UAVs like the Global Hawk, Fire Scout and Taranis are leveraging embedded computer processing to achieve ever greater levels of autonomous operation.

Jeff Child,
Editor-in-Chief

Late last month the Global Hawk made history when an RQ-4 version of the UAV completed a flight of 33.1 hours at altitudes up to 60,000 feet, setting an endurance record for a full-scale UAV. In doing so, the aircraft—designated AF-8, the first Global Hawk Block 20—surpassed both the official and unofficial world un-refueled endurance records for operational unmanned airplanes previously held by the Global Hawk Block 10 variant.

As impressive as that milestone was for the decade-old Global Hawk platform, perhaps even more impressive are the changes going on inside the large UAVs—like Global Hawk, Predator, Fire Scout, Taranis and others. If there's a trend that exemplifies the future goals for large UAVs, it's toward payloads that enable ever greater autonomy for the UAV and its mission. Autonomy in this context doesn't mean taking remote pilots out of the loop—that sort of independence is still a long way off. Rather, the trend is twofold: Increasing the detailed aspects of a UAV's mission that it controls by itself, and boosting the amount of data and image processing done by the UAV payload. By doing more of that processing on the UAV, a more refined set of information can be transmitted to war fighters on the ground.

Figure 1

An RQ-4 Block 20 version of Global Hawk completed a flight of 33.1 hours at altitudes up to 60,000 feet, setting an endurance record for a full-scale UAV. That meant breaking the official and unofficial world un-refueled endurance records for operational unmanned airplanes previously held by the Global Hawk Block 10 variant.

For the near-term, U.S. Military strategy entails relaying almost all UAV captured data to the ground and to process it for interpretation and de-

cision making. But eventually—thanks to the boost in onboard processing muscle—UAVs should be able to relay the results of their data to the ground for decision making. The benefit is reduced reliance on data link rates in certain applications, particularly imagery collection. Tasked to capture and download secure, encrypted surveillance data, today's advanced surveillance UAVs require a lot of communications overhead. If processing of data and decision making can be performed onboard the UAV itself rather than performed via a communication link with the ground, the more efficiently the craft can be used.

In today's UAVs, image formation is done in the air and then sent down. For payloads of the future, the trend is toward fusing data and sending down just things that are different than the established data base—or some other way of compressing and fusing the information. All of this helps overcome the defining constraint for these systems, which is: the limitations of data link bandwidth.

FPGAs Collapse Board Count

Next-generation UAVs are replacing the multiprocessing of big, power-hungry boards based on general-purpose processors like the PowerPC-based boards, with more integrated boards sporting FPGAs. The original Global Hawk, for example, embedded around 40 processor boards. Today's payloads replaced around 30 of those boards with a couple of FPGA-based cards.

It isn't just straight processing integration that the FPGAs provide. They're most efficient at the DSP-kinds of functions done on-board like radar processing and SIGINT. According to software developers involved in the project, when the Global Hawk used a multicomputer comprised only of PowerPC Altivecs, it was inefficient when it came to many of the computing tasks. The new thinking is to let FPGAs concentrate operations like repetitive convolutions—essentially data reduction and manipulation, which take up around three quarters of the total processing in these systems. That leaves the PowerPC processors to focus on data-dependent "intelligent" operations—which general-purpose processors like the PowerPC are good at.

Figure 2

Provided by Curtiss-Wright, the Sensor Management Unit (SMU) deployed on the Global Hawk facilitates data management from all of Global Hawk's airborne payload sensors via a wide range interface I/O including Fibre Channel, Gigabit Ethernet, ECL, 1553, RS-422/485/232 and RS-170 Video packaged with multi-node processing units in an air-cooled, rugged chassis.

While the move toward FPGA-based boards allowed Global Hawk payload designers to chop down the number of boards needed dramatically, they still face a nagging mismatch on the I/O side. Large UAVs like the Global Hawk are packed with a staggering amount and variety of I/O—everything from 1553 to RS-422 and RS-232. That means a smaller set of boards must somehow accommodate the same amount of front-panel I/O. System developers are looking at ways to leverage switch fabric solutions to ease that burden.

Road Toward IP-Centric Ops

Even as large UAVs muscle up their processing payloads and sensor counts, there's a parallel drive to network all that acquired and processed data within the system between subsystem nodes. That's driving the sensor management networks on-board to boost their bandwidth and keep the data flowing. Meanwhile, the format of the data is equally critical as the U.S. Military transitions to a fully IP-based network-centric capability. The current version of the Global Hawk includes a Sensor Management Unit (SMU) (Figure 1), which provides a common interface between the sensor payloads and the rest of the aircraft systems. This enables sensor payloads to be easily redefined and changed without impacting the Operational Flight Program (OFP) and other subsystems in the aircraft.

Provided by Curtiss-Wright, the SMU deployed on the Global Hawk facilitates data management from all of Global Hawk's airborne payload sensors via a wide range interface I/O including Fibre Channel, Gigabit Ethernet, ECL, 1553, RS-422/485/232 and RS-170 Video packaged with multi-node processing units in an air-cooled, rugged chassis. The SMU is designed to support both legacy interfaces and high-speed technologically advanced sensor/payloads. The SMU's job is to gather, manage, store and re-transmit critical data to ground stations quickly and reliably.

The SMU system comprises advanced multi-node processor boards, various legacy and high-speed interfaces, onboard Solid-State storage, an optional video compression board and a backplane that supports both CompactPCI and VME 6U boards. The SMU system's backplane features a fabric interconnect between the different bus architectures and high-speed processing nodes, which enables flexible and optimized data transfer for parallel processing to meet high bandwidth requirements.

The SMU packetizes the data that moves from system to system or within the system; all the systems it connects to can be tied together with a fabric such as switched Gbit Ethernet. Because it's Internet Protocol (IP)-based, the subsystem blocks can be virtually linked to each other on board the UAV as well as to systems anywhere in the world. The ultimate goal is to leverage the advantages of IPv6. With IPv6, a centralized router is no longer needed, and organizations like the U.S. Military can have a huge network that's spread around the world, without the need for different subnets.

Among the most advanced UAV projects underway is a new platform called Taranis. Taranis (Figure 3) is a technology demonstrator program,

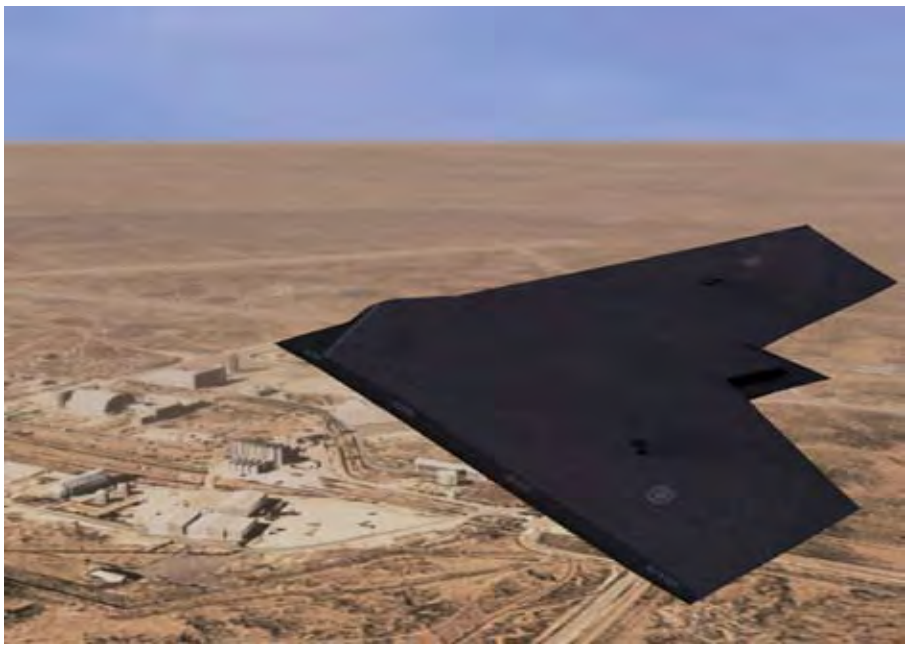


Figure 3

The Taranis UAV is a technology demonstrator program whose computing payload will be able to autonomously control the aircraft to taxi, take off, and navigate its way to a search area while reacting to any threats or other events. QinetiQ is providing the Reasoning Layer of the Autonomy Mission, which runs complex decision-making and optimization algorithms on an embedded processor.

with BAE Systems as the industry lead and prime contractor, and other industry partners comprising QinetiQ, Rolls-Royce and Smiths Aerospace. As the largest UAV yet built in the UK, its computing payload will be able to autonomously control the aircraft to taxi, take off, and navigate its way to a search area while reacting to any threats or other events. It will then route its way around the search area in whichever way it wants to, locate the target, and then use its sensor system to transmit a series of images and views back to the operator to confirm it is the target to be attacked. Then, once it has been authorized to do so, it autonomously attacks that target, routes its way back home, lands and taxies back. Ground testing is expected to take place in early 2009, with the first flight trials taking place in 2010.

QinetiQ is providing the Reasoning Layer of the Autonomy Mission System for Taranis. The system makes the high-level plans that control the flight path and sensor usage to achieve a mission. The Taranis Reasoning Layer needs to run complex decision-making and optimization algorithms on an embedded processor. QinetiQ chose Aonix's PERC Ultra virtual machine for the system. PERC enables existing Java code and libraries to be used in an embedded environment while providing the necessary support for soft real-time operation. Following extensive evaluation, QinetiQ found PERC Ultra as the most practical solution to meet the project requirements on its chosen embedded processor and real-time operating system. QinetiQ needed access to PERC's efficient AOT compilation and static loading capabilities as well as the ability to connect to existing libraries of C++ routines.

Last fall BAE Systems selected GE Fanuc to participate in the Taranis UAV Program. GE Fanuc's RT4 was selected for deployment within the demonstrator program. The RT4 was designed and manufactured by the then Radstone Embedded Computing, which was acquired by GE Fanuc Embedded Systems. The RT4 is a small form factor CompactPCI-based rugged compute node with four conduction-cooled 3U slots, one of which is pre-loaded with the IMP2A single board computer. It features a high-integrity bonded section chassis construction to provide exceptional strength, while the I/O connector panel and backplane are formed as a single, removable assembly for ease of maintenance.

Fire Scout UAV Adds Radar to its Payload

Another UAV design that's pushing the envelope of complexity and control, is the Fire Scout Vertical Takeoff and Landing Tactical Unmanned Aerial Vehicle (VTUAV). While not technically a Joint Army/Navy program, the two branches are cooperating closely on it. The Army has selected Fire Scout as its Class IV UAV for its Future Combat Systems program. The Navy Fire Scout (Figure 4), much further along in its development, achieved first flight in January 2006. The design was a ground-breaking system because it marked the first time a UAV performed vertical landings on a moving ship without a pilot controlling the aircraft.

Accomplishing that required a level of embedded computing power beyond that of any previous UAV. Embedded computers and the payload interface unit aboard the MQ-8B Fire Scout are 3U CompactPCI boards supplied by GE Fanuc Embedded Systems. Offering size, weight and power advantages compared to 6U VME, 3U CompactPCI has become a popular choice for UAV designs. Also on the air vehicle are three Rockwell ARC-210 Radios, with a growth path that accommodates substituting those for JTRS Radios when they become available. Other onboard avionics are Raytheon's Tactical Control System (TCS) and BAE Systems' IFF (Identification Friend or Foe) system.

Last month, Northrop Grumman revealed that radar will be incorporated onto the MQ-8B. The Navy has decided to commit funds in 2009 for those efforts.

Northrop Grumman first demonstrated radar capability on the RQ-8A Fire Scout in 2003 using a General Atomics Lynx Radar. That demonstration carried both radar and an electro-optical/infrared system. The same demonstration will take place on the MQ-8B Fire Scout this year on a company-owned Fire Scout using a non-developmental Telephonics RDR-1700B maritime surveillance and imaging radar.

According to Northrop Grumman, the purpose of the demonstration is to show enhanced Fire Scout operational utility while confirming the assessment of a need for radar. Radar would not only benefit the U.S. Navy, but would also be beneficial to other services interested in Fire Scout. According to the current U.S. Navy schedule, the Navy will conduct Technical Evaluation on the Fire Scout in the fall of 2008, and Operational Evaluation (OpEval) in the spring of 2009. The Fire Scout will reach Initial Operating Capability soon after OpEval in 2009. ■■

Figure 4

Northrop Grumman will be incorporating radar onto the MQ-8B Fire Scout. A demonstrator carrying both radar and an electro-optical/infrared system will take place on the MQ-8B Fire Scout this year on a company-owned Fire Scout using a non-developmental Telephonics RDR-1700B maritime surveillance and imaging radar.

Aonix
San Diego, CA.
(858) 457-2700.
[www.aonix.com].

Curtiss-Wright Controls Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

GE Fanuc Embedded Systems
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

Tech Recon

ATCA-Based Military Systems

ATCA Meets Needs of Mission-Critical Designs

Although created for the telecom market, ATCA is well suited for defense and aerospace industries as they turn to IP networks and real-time data, voice and media transfers over IP.

Dan Leih, Product Marketing Manager ATCA
Emerson Network Power, Embedded Computing

Many military and avionics communications systems are switching to IP-based networking for their framework. This has opened a new opportunity for design teams to speed development and deployment of mission-critical communications systems by leveraging standards-based commercial products. The Advanced Telecommunications Computing Architecture (ATCA) is one such commercial standard, created for the design of high-reliability telecommunications systems, which can also serve military and avionics needs.

New Pressures on Mil Systems Designers

Military communications system designs are under pressure to keep development and system costs contained. As a result, the defense and aerospace industries are turning to an all-IP network approach to system design, seeking to leverage the commercial technologies and design expertise that have evolved in support of the Internet. This approach gives system developers access to a full range of communications channel characteristics, including the guaranteed data transfer characteristics of the classic Internet Protocol (IP) and the real-time data voice and media transfers available through IP streaming protocols.

Figure 1

Shown here is an ATCA blade using an AMC to handle compute or I/O functions, adding flexibility to the hardware design.

At the same time, military systems face an urgent need for rapid development so that emerging technologies and new solutions to field challenges can become available for use in existing theaters of operation. To meet this need, system designs must extensively leverage existing hardware and legacy software. There is not enough time for creation of fully custom designs. Such re-use of existing designs can help speed both system development and time to production.

Yet such use of commercial technology and designs must address the special requirements of mission-critical system design. Two critical requirements are high reliability, to limit the occurrence of failures, and high availability in the form of redundancies with fail-over and an ability to perform hot-swap replacement of system units. In addition, these systems typically must operate in harsh environments, including extreme temperatures as well as mechanical shock and vibration.

Telco and Mission-Critical Needs Align

Perhaps surprisingly, there is a commercial application that shares many of these same requirements: telecommunications. Commercial telco systems are also switching to all-IP networks to deliver voice, data and multimedia to consumers at the lowest possible cost. They have a need for high reliability and hot-swap replacement in order to maintain 99.999% (five nines) service availability. They even face a relatively harsh—for commercial systems—operating environment, with the typical installation site a small, over-crowded concrete building with limited ventilation.

The telecommunications industry has evolved a design approach that allows them to create systems quickly at relatively low cost by basing their designs on open industry specifications. Open industry specifications allow many independent hardware and software vendors to develop products that will be interoperable when assembled into a full system. This fosters

Don't Settle For the Slow Lane

0 to1.5 GBytes in *One Second* Flat

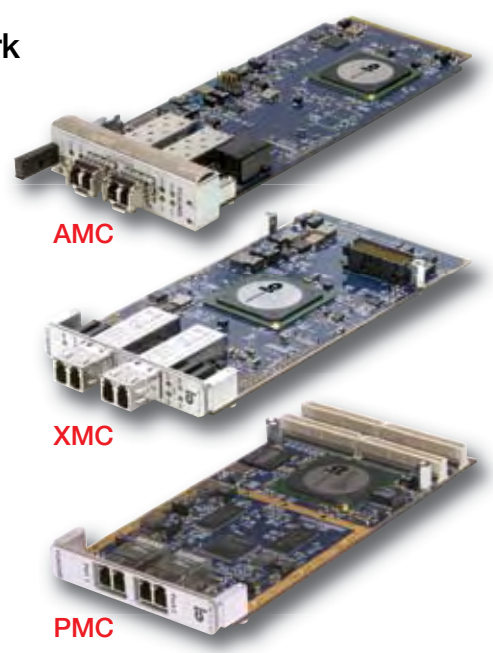
4Gb Fibre Channel – Delivering Performance to Network and Storage Applications

You design-in Fibre Channel for performance and now you can have it —

- Extensive driver and software library support
- AMC, XMC & PMC form factors
- Comprehensive storage and networking protocol support
- 1.5GBytes/second sustained transfer rate
- 4/2/1Gbps dual channel

Critical I/O offers an unparalleled level of engineering expertise and integration support to guide your team down the winding Fibre Channel road toward maximum performance with minimum risk.

Make sure your systems are ready for the long haul. Contact Critical I/O about 4Gb Fibre Channel for embedded systems — today.



CRITICAL IO

www.criticalio.com

competition, which stimulates innovation and drives down cost, while allowing the telco system developers to quickly respond to changing market needs. In addition, the approach gives vendors a broad market for their products, which enables them to attain production volumes that help lower costs and ensure off-the-shelf availability.

ATCA is a key open industry specification for telecommunications system design that can be readily adapted to use in mission-critical military and aerospace communications systems. The specification is stable, well established and well supported with more than one hundred vendors and system integrator companies offering conforming products and design services. ATCA incorporates all the features that mission-critical system design requires and supports both rapid development and customization to meet unique system needs.

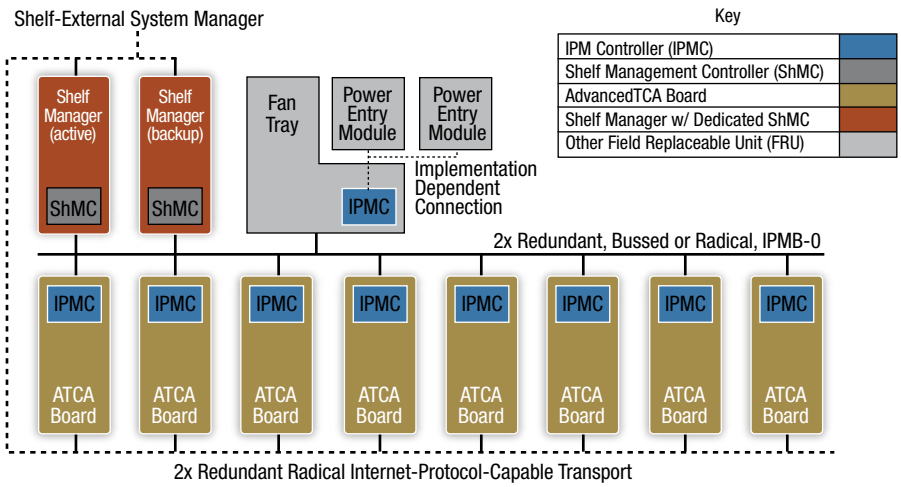


Figure 2

ATCA system management provides system sensing and module-level failure detection as well as controls that enable electronic keying and hot-swap replacement.

Multi-Protocol Fabric Backplane

Like the well-known VME system approach, ATCA uses a modular card and cage structure that allows developers to build systems by combining cards containing the needed functionality. Unlike VME, however, it uses a serial communications bus structure for higher system bandwidth, combining a 10 Gbit/s, multi-protocol switched fabric backplane with large form factor cards and integrated system management specifically to support the creation of high-density, high-performance and high-availability networking systems. Its backplane provides full mesh or dual star connectivity to simplify redundant system design, and can use IP as its native protocol to simplify connection of the ATCA-based design to other IP-based equipment without the need for buffers or protocol adapters.

The large 8U Euro-style cards in ATCA provide gas-tight connections to high-density backplane connectors and can draw as much as 200W from system power to support complex and computationally powerful designs. Processor cards are available today featuring all major processor architectures. Specialized system cards provide application-specific functions such as switching, media processing or storage. One such card, called an AMC carrier, uses as many as four plug-in Advanced Mezzanine Card (AMC) modules to provide compute functions or unique I/O interfaces, adding another layer of mix-and-match configurability to an ATCA system design (Figure 1). These AMC modules are also field-replaceable units and can be utilized without a carrier card, plugging directly into a MicroTCA backplane to create

PC/104-*PLUS*
Family

PMC
Family

cPCI
Family

WHEN RELIABILITY COUNTS...

Four decades of time-proven ***reliability***, thousands of design-ins, and long life cycle support, make DDC the one MIL-STD-1553 and ARINC 429 company you can rely on for generations to come.

DDC®

©Data Device Corporation

Toll Free: 1-800-DDC-5757 **www.ddc-web.com**

a compact design alternative that uses much of the same hardware and software that would go into a larger ATCA design.

System Management Built Into ATCA

For its built-in system management, ATCA utilizes the Integrated Peripheral Management Interface (IPMI) to actively monitor and control individual ATCA blades with an I^2C-based physical link between chassis management and board-level FRUs (field-replaceable units) (Figure 2). Through this interface, chassis management can read sensors to monitor physical system health characteristics such as voltages, fan speeds, temperatures and power supply status. Chassis management can also utilize IPMI for automatic event notification, to initiate remote shut-down/restart of modules, and to dynamically allocate power to individual blades, which helps designers optimize system-wide power consumption and cooling.

One important function of the system manager is to prevent incompatible or failed devices from harming each other or disrupting communication in the system. It is able to provide this service because it controls two power feeds to each card interface or AMC module: management power and payload power. Management power feeds the circuits that interface with the carrier manager, allowing the card or module to interact with the manager and report its functions, connections and status before being allowed to connect with the backplane. Payload power feeds the rest of the module, including its backplane interfaces. If there is a malfunction, the system manager simply disables the module's payload power to prevent it from interacting with the backplane fabric.

This ability to disable individual AMC modules or ATCA blades is one of many high-availability hooks built into ATCA. The system can turn off and on modules for hot-swap replacement or to provide a fail-over function by activating a redundant module when one fails. This support for system fail-over redundancy includes power supplies and cooling units as well. Software for implementing such high-availability system operation in an ATCA design—OpenSAF—is commercially available and, like ATCA hardware, is based on open specifications.

Automated Config and Control

ATCA was designed to address the needs of telecommunications system design, but maps well to the needs of mission-critical military systems. ATCA's system management, for example, provides automated configuration and control of system elements including system monitoring, failure detection and electronic keying to prevent incorrect board insertion. System reliability issues are addressed with well-specified thermal management, power margin and EMI shielding requirements. Hot-swap capability for field-replaceable modules, blades, fans and power supplies is built into the specification, giving de-

Looking for a First-Class CompactPCI® Solution that Really Delivers?

Whether you are seeking to reduce development time, advance communications infrastructures, increase efficiencies, or develop high availability solutions, our PICMG® 2.16 products deliver the first-class performance, speed, and reliability required to complete your mission-critical objectives.

By originating the PICMG 2.16 specification, we revolutionized CompactPCI® to meet the need for increased bandwidth in next-generation platforms. We continue to lead today by offering a wide range of 2.16-compatible platforms and blades that provide the building blocks for reliable, high-performance systems.

Your first-class solution is here. Call now, or visit us at www.pt.com today for your upgrade.

Get onboard today
with our CompactPCI® whitepaper!

CompactPCI + Ethernet
The Winning Alternative to Aging VMEbus Systems

Download at: **www.pt.com/whitepaper**

PERFORMANCE TECHNOLOGIES

CPC5564
64-Bit Opteron™ Single Board Computer

CPC6622
24 1Gb and 2 10Gb Ethernet Switch

CPC324
24-Port T1/E1/J1 TDM/IP Edge Processor

CPC5900
RAID-ready SATA Storage Blade

Phone: 585.256.0200 ◆ www.pt.com ◆ E-mail: info-request@pt.com

signers the functions they need to implement fail-over redundancy, load sharing and other high-reliability schemes.

Open Systems Speed Development

All these hardware functions are available to designers as stock items from a variety of vendors. Linux and real-time operating system software from vendors such as Wind River, and high-availability middleware are available off-the-shelf. The result is that most of the foundation needs of mission-critical system designs are already implemented, even down to built-in temperature sensors in the card cages. The development team needs only to implement their unique system requirements in ATCA-compliant hardware and software to form complete system designs with minimal effort.

One concern that might arise for military system developers is the availability of unique or legacy compute architectures in the ATCA format. This issue is easily addressed within the bounds of the ATCA specification, however. The board, system management and backplane interface specifications are all independent of the underlying compute architecture. This allows the system to support virtually any legacy or unique compute architecture the developer requires, including DSPs.

The reliability of commercial hardware may also be a concern for military system designers. Unlike consumer manufacturers that have cost as their key factor, however, the hardware vendors for telco system elements focus on providing high reliability. Emerson Network Power, for example, performs a detailed reliability and failure analysis of its board designs, looking at the architecture, interconnects, power and cooling in a reference installation. This analysis both provides a detailed measure of board reliability as well as identifying the most likely failure modes so that system designers can prepare response strategies.

Adapting to Military Environments

Harsh operating environments represent a third concern for military system designers looking to utilize commercial hardware, and the ATCA specification goes a long way toward addressing those concerns. Because commercial telco installations are often in overheated closets or windowless concrete buildings, the ATCA specification addresses thermal management by defining forced-air-cooling requirements that card cages, cards and cable placements must meet, and many boards are fabricated using extended-temperature components. This makes off-the-shelf hardware suitable for prototyping and early field trials at least, allowing software development and qualification testing to occur before ruggedized boards are fabricated. Extended-temperature commercial equipment may also be acceptable for use in the relatively benign environments of shipboard and stationary installations.

For other installations, however, commercial ATCA hardware may need some

ACROMAG FPGA I/O SOLUTIONS

Simply Powerful. Powerfully Simple.

VIRTEX™ 5

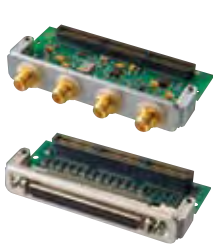
High-performance FPGA I/O designed for faster and easier development.

Only Acromag gives you a reconfigurable FPGA wrapped with just the features you need for fast and easy implementation. These PMC modules provide a high-speed I/O interface with plenty of memory for efficient data handling.

- Virtex-5 FPGAs (VLX155T/110T/85T or VSX95T) are optimized for logic or DSP
- Two banks of high speed 32M x 16-bit DDR2 SDRAM handle high volumes of data
- Two banks of 256K x 32-bit dual-port SRAM optimize DMA transfer to the bus
- PCI-X 133MHz 64-bit interface ensures fast data throughput
- Engineering Design Kit speeds development of custom FPGA applications.

Plug-in I/O cards extend the I/O capabilities

AXM I/O extension modules expand interface support for a wide variety of analog and digital I/O signals.



Affordable FPGA-based I/O for all your projects

Acromag's full line of industry pack and PMC modules feature Xilinx FPGAs at a range of price and performance points. Why settle for generic I/O when you can cost-effectively design just what you need?

For details on the fastest and easiest way to develop FPGA I/O visit

AcromagEmbedded.com, or call 1-877-295-7084

Acromag®
THE LEADER IN INDUSTRIAL I/O

acromagembedded.com • solutions@acromag.com • 877-295-7084 or 248-295-0310

adaptation before seeing field use. Fortunately, third-party services are available that will ruggedize commercial boards to prepare them for harsh environmental conditions. One such service provider, ACT Technico, offers a multi-stage ruggedization strategy that addresses both temperature and shock/vibration needs. ACT/Technico, an authorized Emerson Value Added Integrator, has a ruggedization program that extends the temperature range of off-the-shelf Emerson boards from the warranted limit of 0° to +55°C, up to -20° to +70°C and in some cases beyond.

ACT/Technico processes the commercial board through functional temperature screening to verify operation over the extended temperature range. Rigorous shock and vibration requirements can often be met through minor modifications to COTS boards, as well as conformal coating for salt spray environments. ACT/Technico also manages a ruggedized board's warranty, by serving as the return depot, reducing the customer's risk.

Similar to Mission-Critical Comms Needs

Even if some adaptation is required, the benefits of using commercial ATCA hardware are significant. Because of the similarity in needs for mission-critical communications networks and commercial telecommunications networks, most of the functional elements for a mission-critical design have already been addressed in the ATCA specification and implemented in ATCA-compliant hardware and software. This eliminates a major segment of the system design task and shortens development time.

The wide range of inter-operable products available from multiple vendors means that most of the system elements a designer will need are readily available off-the-shelf for prototyping, shortening development time even further. Where differences in military and commercial operating environments exist, use of an adaptation service can make ATCA-compliant commercial hardware suitable for military application. Custom design of individual boards is also an option.

The ATCA design strategy, then, addresses all the key functional and operational needs of mission-critical military communications systems. It offers the flexibility to meet unique system needs while providing all the required base features of system management and high availability. The strategy supports rapid development and deployment, speeds the incorporation of new technologies as they become available, and lowers production costs to approach commercial levels. ATCA thus provides a new opportunity for developers to address the increasingly demanding needs of military and avionics system design. ■■

Emerson Network Power,
Embedded Computing
Tempe, AZ.
(800) 759-1107.
[www.emersonnetworkpower.com].

We Simplify Technology

CORE SYSTEMS

Reliable operation in severe environments

- Integrates hardware mechanically, electrically and thermally
- Fanless, total thermal solution
- Mini PCI & PC/104 expansion
- MIL–810F, EN50155 available
- Installed Windows® XPe or Linux available
- Virtually indestructible mobile power supply
- NEMA 4X
- –40° to 85° C

- Transportation
- Mining vehicles
- Outdoor kiosks
- Industrial servers

- Digital signage
- Military and police
- Traffic management
- Digital video surveillance
- Asset management

303–430–1500

OCTAGON SYSTEMS

www.octagonsystems.com

Tech Recon

ATCA-Based Military Systems

ATCA Carves Out Niche in Mil Applications

ATCA has made impressive inroads into the military market mindshare. Its communications bandwidth and high-availability features help seal the deal.

David Pursley, Field Applications Engineer
Kontron America

ATCA has become a preferred form factor for certain types of military and aerospace applications, despite its origins as a telecommunications architecture. ATCA and its smaller cousin MicroTCA have made it into applications outside of the bases and depots and can now be found in everything from shelters to aircraft.

In contrast to the majority of military applications from five or ten years ago, today's military programs, such as FCS (Future Combat Systems), JTRS (Joint Tactical Radio System) and WIN-T (Warfighter Information Network – Tactical), are heavily communication-centric. It's not surprising therefore that the embedded computing architectures of yesterday are hard pressed to keep pace with the demanding communication bandwidth requirements of today's applications.

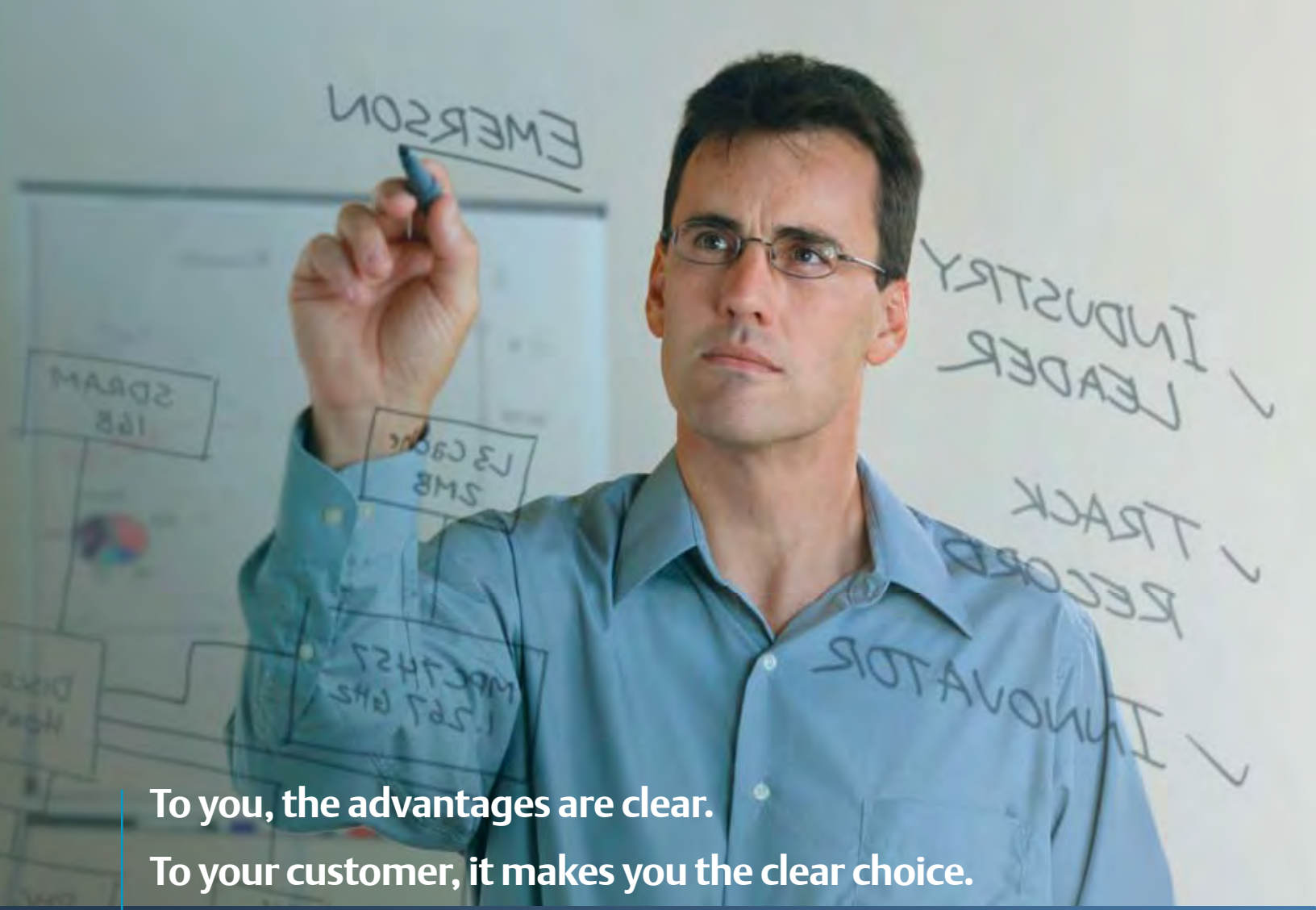
VME and CompactPCI, for example, while still viable for many applications, do not support the processing and communication bandwidth required for these applications. Switched-fabric extensions to these architectures (VITA 31, VITA 41 and PICMG 2.16) offer more bandwidth, but still do not meet the communication demands inherent in the new advanced programs. The ATCA standard has risen to address this issue. Ratified in 2002 as PICMG 3.0, ATCA offers extremely high communication bandwidth, extremely high processing capacity, and up to five nines availability (99.999% uptime).

Although originally designed as a telecom standard, design teams have deployed ATCA into a wide range of application spaces, including defense, government, aerospace and medical. Applications in these spaces present some similar requirements, including the need for a very dense computing platform with high communication bandwidth in a fairly rugged form factor.

The biggest advantages of ATCA are its extremely high computing power, high communication bandwidth and high availability. Up to 14 blades can exist on a single backplane, and each blade can

Figure 1

The Kontron AT8030 (left) has three Intel dual-core processors on a single blade, and its mezzanine can be populated with an AMC such as a fourth processor or a peripheral such as the AM4500 SATA storage AMC (center). The flexibility of ATCA can be realized via Kontron's AT8404 (right), which allows any four AMCs to be used in order to best meet the project requirements.



To you, the advantages are clear.

To your customer, it makes you the clear choice.

Emerson Network Power is now clearly the leading provider of embedded computing solutions.

From platforms, blades and modules, to software and services, Emerson's industry-leading technology portfolio is ready to help solve your customers' most demanding applications. Make our AdvancedTCA®, MicroTCA™, AdvancedMC™, CompactPCI®, Processor PMC, VMEbus and OpenSAF™ standards-based products your first choice.

See how Emerson Network Power can help you build a clear advantage.

Go to www.EmersonNetworkPower.com/EmbeddedComputing

Standards-based Embedded Computing

Just another reason why Emerson Network Power is the global leader in enabling Business-Critical Continuity™

The Embedded Communications Computing business of Motorola is now a business of Emerson Network Power.

EMERSON™
Network Power

EMERSON. CONSIDER IT SOLVED.™

typically have up to four CPUs on board. Combined, this allows up to 56 (multicore) processors in an 8U x 19-inch rackmount system.

The processing blades communicate over the backplane via high-bandwidth channels, typically Gbit Ethernet or 10 Gbit Ethernet, in either a star, dual star, or full mesh topology. Peripherals such as storage drives, graphics cards and security modules also communicate over the backplane, typically via PCI Express, Serial Rapid IO, SATA, or SAS. These communication lanes can also be redundant.

The redundancy of the dual star and full mesh topologies is a key factor in making ATCA systems highly available. There is no single point of failure in a properly designed redundant ATCA system. Other features of ATCA that support high availability include the ability to hot swap all LRUs (line-replaceable units), redundant IPMI (Intelligent Platform Management Interface) buses for health monitoring, and shelf management.

ATCA provides very high compute density blades communicating over 10 Gigabit Ethernet. For example, Figure 1 shows the Kontron AT8030 with three Intel dual-core processors on a single blade, and its mezzanine can be populated with an AMC such as a fourth processor or a peripheral such as the AM4500 SATA storage AMC. The flexibility of ATCA can be realized via Kontron's AT8404, which allows any four AMCs to be used in order to best meet the project requirements.

High Availability a Requirement

In the past, high availability was not a requirement for military systems, but it is growing in desirability for military applications. High availability in this context means maximizing system uptime via redundancy and the ability to "heal" it in the field. The features above, if properly leveraged through judicious use of middleware and/or application support, can provide systems with up to five nines (0.99999) availability.

ATCA systems are more than rugged enough for benign environments, such as those in ground installations or on airborne platforms. ATCA boards and systems are designed to meet NEBS Level 3, which includes requirements such as thermal margins, fire suppression, emissions, and the ability to remain operational during a severe earthquake.

Figure 2

The P-8A Poseidon, based on the Boeing 737-800, and other military derivative aircraft use ATCA because of its processing power and relative ruggedness.

Also advantageous to defense applications is ATCA's inherent separation of control plane and data plane communications. The control plane communicates via Gigabit Ethernet, while the data plane can use higher bandwidth, such as 10 Gigabit Ethernet. The control and data planes have separate communication ports on each blade in the system, and control and data communications are separately and independently switched by the switch blades in an ATCA system.

It should also be noted that ATCA is highly scalable, which makes it a versatile solution for a number of applications. Beyond being scalable in the number of boards (configurations ranging from 2 boards to 14 boards are typical), ATCA is also scalable in terms of functionality. For example, if high availability is not required, some redundancy and/or middleware functionality can be removed, reducing the cost of the system.

As an extreme example of ATCA's flexibility, ATCA's mezzanine cards (AdvancedMCs or AMCs, for short) can be used as line cards in the smaller 2U MicroTCA platform. MicroTCA is basically a smaller version of ATCA, representing a smaller form factor and often lower cost for applications that do not require the compute density of ATCA systems.

ATCA's flexibility has made it a successful platform for a wide variety of application spaces, including defense applications. For example, ATCA is being used in military derivative aircraft programs, datacenter servers, and for multiple programs best categorized as server consolidation programs.

ATCA in Military Derivative Aircraft

Military derivative aircraft were originally designed as commercial vehicles and then retrofitted or modified to be a military platform. One example of military derivative aircraft using ATCA is Boeing's P-8A Poseidon program. The P-8A Poseidon (Figure 2) program modifies a Boeing 737-800 aircraft to make a long-range anti-submarine warfare, anti-surface warfare, intelligence, surveillance and reconnaissance aircraft capable of broad-area, maritime and littoral operations. These capabilities require a great amount of computational power, and it needs to be done in a fairly limited thermal envelope and footprint. Additionally, the systems need to be rugged enough to survive and operate during wartime operations.

ATCA is a logical choice for networked datacenter servers, which can be characterized as high-bandwidth network infrastructure systems. Essentially, these systems ensure that data coming in one port make it to the correct outbound port. These servers often also include functionality like communication priority management, security management and transcoding data, voice, or video from one format to another.

For example, Lockheed Martin selected ATCA for use in its Wideband Data Subsystem (WDS). This system, which is designed to be used in multiple programs, executes four distinct processing functions while translating high-speed serial data to a computer-readable

format. Essential to this capability is the requirement to route 10 million 2,000 byte packets per second between the processing blades, a task well-suited to ATCA because of its 10 Gbit communication infrastructure.

It should be no surprise that ATCA is being used for these applications by the military community, as this usage is very close to its telecommunications roots. In fact, in many cases a military ATCA datacenter server located in a base, depot, or shelter is nearly indistinguishable from its cousin sitting in a central Telco office. This is especially true because of the recent push for military programs to use infrastructure based on commercial communication technologies such as Gbit Ethernet, Voice over IP (VoIP), 802.11 wireless standards and WiMax. ATCA is a well-proven technology for these applications.

It is also worth mentioning that significant portions of the WIN-T program are using the MicroTCA architecture. MicroTCA uses the ATCA mezzanine cards (AdvancedMCs) as blades in the system. Like these other datacenter applications, WIN-T is a network-centric program so it is not surprising that a network-centric standard such as MicroTCA is in use for this program.

ATCA for Server Consolidation

Because of its high compute density and high availability, the ATCA architecture is being used as a more compact, more reliable, more powerful alternative to a server farm typically implemented as a number of 1U industrial (or commercial) computers. The military's use of ATCA in this paradigm is usually realized in an upgrade project, such as upgrading servers to increase the processing power on submarines, other naval vessels, or non-mobile ground installations. ATCA is a good technical fit for these applications because of its high compute density and relative ruggedness. Its fault tolerance and high availability make ATCA even more attractive for server applications.

However, the driving factor for ATCA in these upgrades is economic and logistical. A centralized ATCA server farm has a lower Total Ownership Cost and smaller logistics impact than the distributed collection of computers—usually VME or commercial server blades—the new servers are replacing.

Maintenance costs are much lower over the lifetime of the program. For example, a typical server upgrade on a naval platform may be replacing a few dozen commercial-grade servers distributed throughout the vessel with a single ATCA server. This means only one set of fans and filters will need to be periodically inspected and replaced, as compared to dozens. Furthermore, the centralized ATCA server will typically be installed in an easily accessible area, while some of the distributed servers on a submarine or aircraft tend to be in less accessible areas. This reduces the amount of labor and turnaround time for each maintenance event.

Future Uses of ATCA and MicroTCA

To date, ATCA has been selected as the platform of choice for military derivative aircraft, datacenter servers and server consolidation programs. Common to these types of programs are requirements for high compute density, very high communication bandwidth, high reliability and a fairly rugged form factor. MicroTCA's smaller form factor makes it a logical choice when similar requirements are needed in space-constrained applications such as smaller shelters or ground vehicles. Also, recent work in the PICMG standards body has been defining ruggedization levels that MicroTCA can attain and suggesting implementations that would allow it to be used in less benign applications. With the increased push toward commercial platforms and communication technologies, it is reasonable to expect that other types of programs will use ATCA and MicroTCA architectures in the near future. ▮▮

Kontron America
Poway, CA.
(858) 677-0877.
[www.us.kontron.com].

System Development

GPP, DSP, FPGA Trade-Offs

FPGA Advances Ignite Signal Processing Rethink

In military radar, SIGINT and similar systems, FPGAs are being used to augment, and sometimes even replace, general-purpose processors or DSPs.

Manuel Uhm, Senior Marketing Manager, Xilinx
Mark Littlefield, Product Marketing Manager, Curtiss-Wright Controls Embedded Computing

FPGAs have long enjoyed a prominent place in embedded systems. Their flexibility and computational performance per watt make them an attractive choice for systems with tough size, weight and power (SWaP) constraints. Until recently, FPGA-based systems were relatively difficult to develop. Typically they required longer development cycles and required more specialized development talent. As a result, the use of FPGAs has been mostly limited to tasks such as front-end stream or image processing—places where either their computational power-per-watt was critical, or when they were needed as the link to legacy buses.

Recent years, however, have witnessed a change in how and where FPGAs are being used. Thanks to vastly larger gate counts, specialized DSP units, embedded processors and high-speed serial links on FPGAs, system developers now have compelling reasons to find new and novel uses for FPGAs in their military embedded systems. FPGAs are being used to augment, and often replace, traditional general-purpose processors (GPPs) or DSPs.

Figure 1

Xilinx's Virtex-5 FXT family combines DSP, embedded processing and high-speed I/O. That combination suits high-performance military applications like radar and SIGINT.

Meanwhile, new development tools from higher-level and more abstract programming languages, as well as frameworks to system-level tools like Simulink from The Mathworks, are beginning to close the ease-of-development gap with microprocessors and DSPs. Driving by all those trends, embedded computer vendors are taking advantage of those FPGA innovations and are beginning to craft products designed with FPGAs specifically targeted for end-user application development. The results along those lines are affecting system development approaches in tough embedded systems such as Radar and SIGINT.

The traditional view holds that FPGAs are best for high-performance computations, DSPs are best for lower-

Get Connected with companies mentioned in this article.
www.cotsjournalonline.com/getconnected

performance signal processing and decision making, and general-purpose processors are best for managing the control plane. While this view generally remains true, the lines are beginning to blur thanks to the emergence of "platform" FPGAs, combined DSP/GPPs and multicore DSP and GPPs.

Multicore GPPs include devices such as the Cell Broadband Engine from IBM and Xeon processors from Intel. The primary means of boosting signal processing performance in GPPs is through the addition of multiple cores, which essentially enables algorithms to be processed in parallel. Ironically, FPGAs have supported this approach for many years now. While it is certainly true that GPPs can provide significant floating-point performance for applications such as radar, the performance comes with a power consumption cost that makes these devices unattractive for SWaP-constrained applications. With GPPs, total power consumption can exceed 100W, making thermal dissipation a major challenge.

One alternative to GPPs is a combined DSP/GPP architecture, an example of which is Texas Instruments' OMAP platform. This approach couples the superior signal processing performance of the DSP with the control plane management advantages of the GPP. To date, these types of devices have been more commonly targeted to lower-power, lower-performance applications such as cell phones and video cameras. Hence, while they tend to be more SWaP-friendly than multicore GPPs, they still lack sufficient performance for applications such as radar and spectral analysis in a SIGINT system.

Platform FPGAs Bring it All Together

A relatively recent development is the introduction of the platform FPGA, which enhances the programmable logic typically found in FPGAs with DSP engines, embedded processor hard cores and other specialized features. An example of this is Xilinx's Virtex-5 FXT family (Figure 1). The Xtreme DSP MAC (multiply-accumulate) engines of the FXT provide the computational horsepower for high-performance signal processing applications like radar and SIGINT in a far more SWaP-friendly fashion.

Because DSP is not an efficient means for implementation of a robust control processor, the FXT adds up to two 440 PowerPC hard-core processors. Capable of running popular real-time operating systems from Green Hills and Wind River, the 440 cores effectively double the device's GPP performance compared to the Virtex-4 FX. Lastly, with up to 24 high-speed transceivers capable of running up to 6.5 Gbits/s, the FXT is especially well

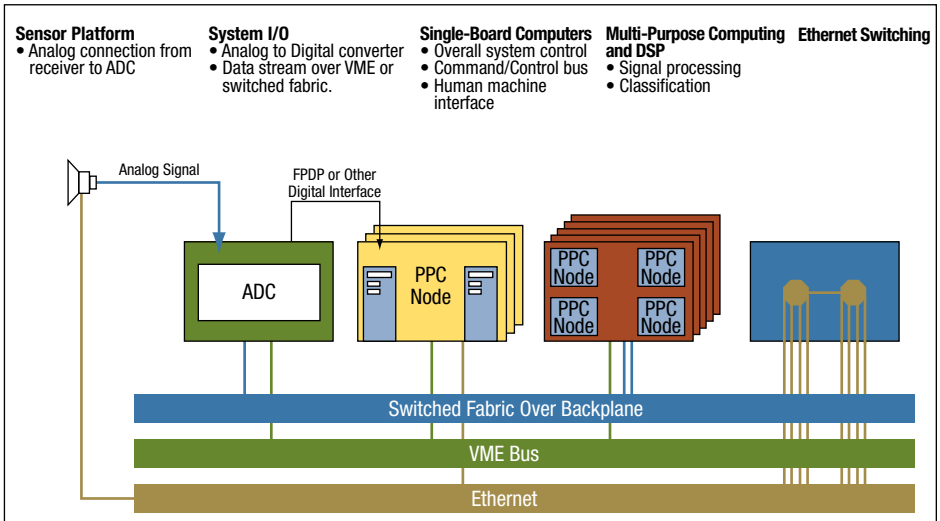


Figure 2a

A traditional view of an advanced embedded signal processing system. Sensor data is sent to an analog-to-digital converter by cable. Raw digital data is then sent to an SBC for distribution to the multicomputer.

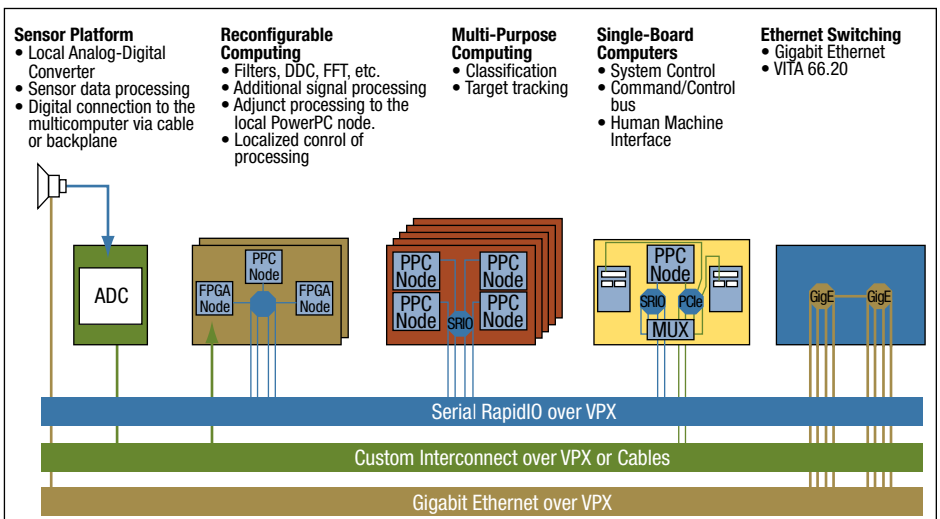


Figure 2b

A revised form of the same system. Sensor data is digitized and pre-processed at the sensor and shipped to the multicomputer over a streaming serial link. Further processing is done on system FPGAs, with a GPP-based multicomputer performing tasks not suited for FPGA processing. Net result is higher system performance with lower SWaP.

RTD Embedded Technologies, Inc.

The Stackable PC Company™

AMD Geode LX 500 MHz

Intel® Pentium® M 1.4 GHz

TI 8000 MIPS dspModules™

cpuModules™
-40 to +85°C

		Intel Pentium M					Intel Celeron						AMD Geode LX	
		CMA157886PX1400HR	CMX158886PX1400HR	CMD158886PX1400HR	CMX158886PX1400HR-BRG	CMD158886PX1400HR-BRG	CME147786CX400HR	CME147786CX650HR	CML147786CX400HR	CML147786CX650HR	CMX147786CX400HR	CMX147786CX650HR	CME136686LX500HR	CME137686LX500HR
Expansion Bus	PC/104 ISA Bus	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI-104 PCI Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4	4		4
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9	9		
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	1400	400	650	400	650	400	650	500	500
	L2 Cache (KB)	2048	2048	2048	2048	2048	256	256	256	256	256	256	16	16
	Intel SpeedStep Technology	✓	✓	✓	✓	✓								
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0		
	Max Onboard DRAM (MB)	512	1024	1024	1024	1024	512	512	512	512	512	512	512	512
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RTD Quick Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Chip (MB)	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096
	Audio		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA
	Digital Video	LVDS	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	LVDS	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	**RS-232/422/485 Ports**	4	4	2	4	2	2	2	2	2	2	2	2	2
	USB Ports	4	2	4	2	4	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1	1	1	1	1	1	1	1	1	1	1	2	1
	ECP Parallel Port		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO (Advanced Digital I/O)	14	18	18	36	36	18	18	18	18	18	18	18	18
	multiPort (aDIO, ECP, FDC)		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

visit www.rtd.com for complete product listing

dspModules™
- Coprocessors
- Accelerators

Specialty I/O
- Pulse Width Modulator
- Incremental Encoder
- Opto-isolated MOSFET

Frame Grabbers
- Single or Multi-channel
- MPEG-2 Compression

Video Controllers
- Analog VGA
- TTL and DVI panels

Communication Modules
- Copper or Fiber Ethernet
- USB 2.0 and FireWire™
- CAN Bus & CAN Spider
- Dual Synchronous Serial
- Quad Serial w/ Ethernet
- Octal PCI Serial

Wireless Telematics
- GSM & GSM-R
- EDGE, GPRS, SMS
- GPS & Wi-Fi

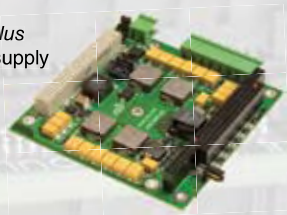
Motion Controllers
- DC Motor Controllers
- Synchro, Resolver, LVDT

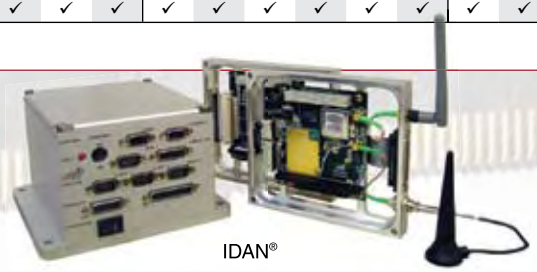
Mass Storage
- 1.8/2.5" IDE & PCMCIA
- CompactFlash

Bridge Modules
- PCIe to PCI
- PCI to ISA

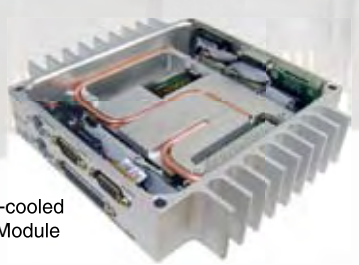
Power Supplies
- PC/104 & PCI/104-*Plus*
- 50/75/83/88/100 Watts
- Wide input range
- ATX Power Supplies
- UPS Backup
- MIL-STD-704/461

PC/104-*Plus*
ATX power supply





IDAN®



Conduction-cooled
IDAN® cpuModule

A Founder of the PC/104 Consortium
ISO9001:2001 Certified

RTD Embedded Technologies, Inc.
103 Innovation Boulevard • State College, Pennsylvania • 16803 • U.S.A.
Phone: 814-234-8087 • Fax: 814-234-5218 • www.rtd.com • sales@rtd.com

www.rtd.com

HighRel PC/104 ISA & PCI Modules and Systems

-40 to +85°C

Autonomous SmartCal™

Wireless Telematics

Frame Grabber

DataModules®
-40 to +85°C

		Smart A/D		Analog I/O					Digital I/O					
		SDM7540HR	SDM8540HR	DM6420HR	DM6430HR	DM7520HR	DM7530HR	DM8530HR	DM6812HR	DM6814/16HR	DM6888HR	DM7820HR	DM8820HR	FPGA7800HR
Bus	Active Bus	PCI	PCI	ISA	ISA	PCI	PCI	PCI	ISA	ISA	ISA	PCI	PCI	PCI
	Passthrough Bus	ISA				ISA	ISA					ISA		ISA
	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓
	McBSP Serial Ports	✓	✓			✓	✓	✓						
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16						
	Differential Inputs	8	8	8	8	8	8	8						
	Max Throughput (kHz)	1250	1250	500	100	1250	500	500						
	Max Resolution (bits)	12	12	12	16	12	16	16						
	Input Ranges/Gains	3/7	3/7	3/4	1/4	3/6	3/3	3/3						
	Autonomous Calibration	✓	✓											
	Data Marker Inputs	3	3	3		3								
Conversions	Channel-Gain Table	1K	1K	1K	1K	1K	1K	1K						
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓						
	A/D FIFO Buffer	8K	8K	8K	8K	8K	8K	8K						
	Sample Counter	✓	✓	✓	✓	✓	✓	✓						
	SyncBus	✓	✓			✓	✓	✓						
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	64	48	48	48
	Bit Programmable I/O	8	8	8	8	8	8	8	24	6/0		48	48	✓‡
	Advanced Interrupts	2	2	2	2	2	2	2	2			2	2	✓‡
	Input FIFO Buffer	8K	8K	8K	8K	8K	8K	8K						
	Versatile Memory Buffer											4M	4M	8MB
	Opto-Isolated Inputs										48			
	Opto-Isolated Outputs										16			
	User Timer/Counters	3	3	2	2	3	3	3	3	3		10	10	6
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓‡
	Incr. Encoders/PWMs									3/9		4/8	4/8	✓‡
Analog Out	Analog Outputs	2	2	2	2	2	2	2						
	Max Throughput (KHz)	200	200	200	100	200	100	100						
	Resolution (bits)	12	12	12	16	12	16	16						
	Output Ranges	4	4	3	1	4	5	5						
	D/A FIFO Buffer	8K	8K			8K	8K	8K						

visit www.rtd.com for complete product listing

‡ User-defined, realizable in FPGA

PC/104-*Plus* AMD Geode LX cpuModule, DataModule & ATX power supply

Conduction-cooled, Hybrid RF/Embedded System

- VHF/UHF receiver
- Multi-band synthesizer
- FPGA Coprocessor
- High-end GPS receiver
- Pentium M cpuModule
- Isolated Power Supply

HiDAN*plus*™

HiDAN™ Systems

- Rugged, watertight enclosure
- Integrated tongue & groove O-ring
- Environmental sealing & EMI suppression
- Structural heat sinks & heat pipes
- Milled aluminum frames with optional heat fins
- MIL cylindrical I/O connectors
- MIL-SPEC paint & shock-mounts optional

IDAN® — Intelligent Data Acquisition Node

- Rugged PC/104 stackable framed modules
- Quick interchangeability and expansion
- Structural heat sinks, cooling fins & heat pipes
- Milled aluminum frames
- Standard PC connectors
- Optional MIL-SPEC paint & shock mounts

HiDAN*plus*™

Radar System Application

- High-end FPGA Board
- MIL Spec A/C Power Supply
- Synchro to Digital Converter
- cpuModule, relayModule and DataModules

HiDAN*plus*™ Systems

- HiDAN with IDAN modularity
- Stackable signal raceway

rtd®
"Accessing the Analog World"

"MIL Value for COTS prices"™

suited to I/O-intensive applications such as beamforming.

New FPGA designs like the FXT provide an opportunity for integrating signal acquisition and processing into a single, compact package suitable for deployment at the sensor (Figure 2). This provides a significant advantage because performing the analog-to-digital conversion, down-conversion and initial signal processing at the sensor maintains an end-to-end digital form of the incoming signal, thus avoiding signal loss or the introduction of noise. This digital form of an intermediate or baseband signal is already proving popular in systems. COTS hardware such as Curtiss-Wright's XMC-E2201 card (Figure 3), with its compact PMC/XMC form factor, high-speed/high-resolution analog-to-digital converters (ADC), onboard digital down converters (DDC) and serial links to the basecard, is an example of a device ideal for this task. When fitted with an FXT FPGA, the XMC-E2201 can capture data, process it, package it, and send it on to later processing stages via PCI, PCI Express, or its high-speed serial links using a number of different protocols, all without direct control from a host processor somewhere in the system.

Figure 3

Curtiss-Wright's XMC-E2201, a rugged and compact high-speed, dual-channel 16-bit digital receiver XMC/PMC mezzanine card, is based on twin Xilinx Virtex-5 FPGAs, combines input bandwidth in excess of 700 MHz, supports analog sampling rates of 160 Msamples/s, signal-to-noise ratio rated at greater than 77 db, and high-spectral purity.

Further Shifts in Traditional Lines

FPGAs have for some time been used to attack what were generally referred to as "massively" parallel problems. Many problems of this class can deliver dramatic improvements in performance, on the order of 10x, 20x or even more, over traditional GPPs or DSPs. Problems that were "merely" parallel may not have seen the same sorts of performance improvements and may not have warranted the steep development investment needed to implement them in an FPGA.

All that said, with the new DSP engines and embedded processors found in current-generation FPGAs, combined with the advances in development tools and frameworks that are beginning to appear, the natural progression is to consider FPGAs for these "merely" parallel problems. Applications such as azimuth and range compression in radar, or wideband spectral analysis or beamforming in SIGINT applications, which were traditionally implemented on GPPs or DSPs, are now being implemented in FPGAs.

The challenge of programming DSP/GPPs also favors the increased use of FPGAs. The recent rapid adoption

YOUR SOURCE FOR MIL-STD-1553B SOLUTIONS

For Over 20 Years, Military Professionals Have Trusted MilesTek's Expertise, Selection and Service for MIL-STD-1553B Components:

Bus Couplers • Cable Assemblies • Connectors • Ethernet Devices • Relay Devices • And More!

MilesTek®
milestek1553.com

866-524-1553
Order by Fax 940-591-7086

EXPERTISE
SELECTION
SERVICE

of multicore processors has introduced new challenges for developers and tool vendors. While splitting an application across multiple processors and coordinating that processing in a real-time system has been common for tough radar and SIGINT applications for some time, the use of multicore processors in these systems tends to have a multiplying effect on system complexity.

Tools vendors are adapting to this challenge, introducing new features to address the added complexity, but they haven't quite caught up with the introduction of ever-larger core counts. The net result is that systems are becoming more difficult to develop. Combined DSP/GPPs face a similar problem insofar as there is no homogeneous integrated development environment. And perhaps an even greater negative impact than the development complexity is the verification and debugging complexity.

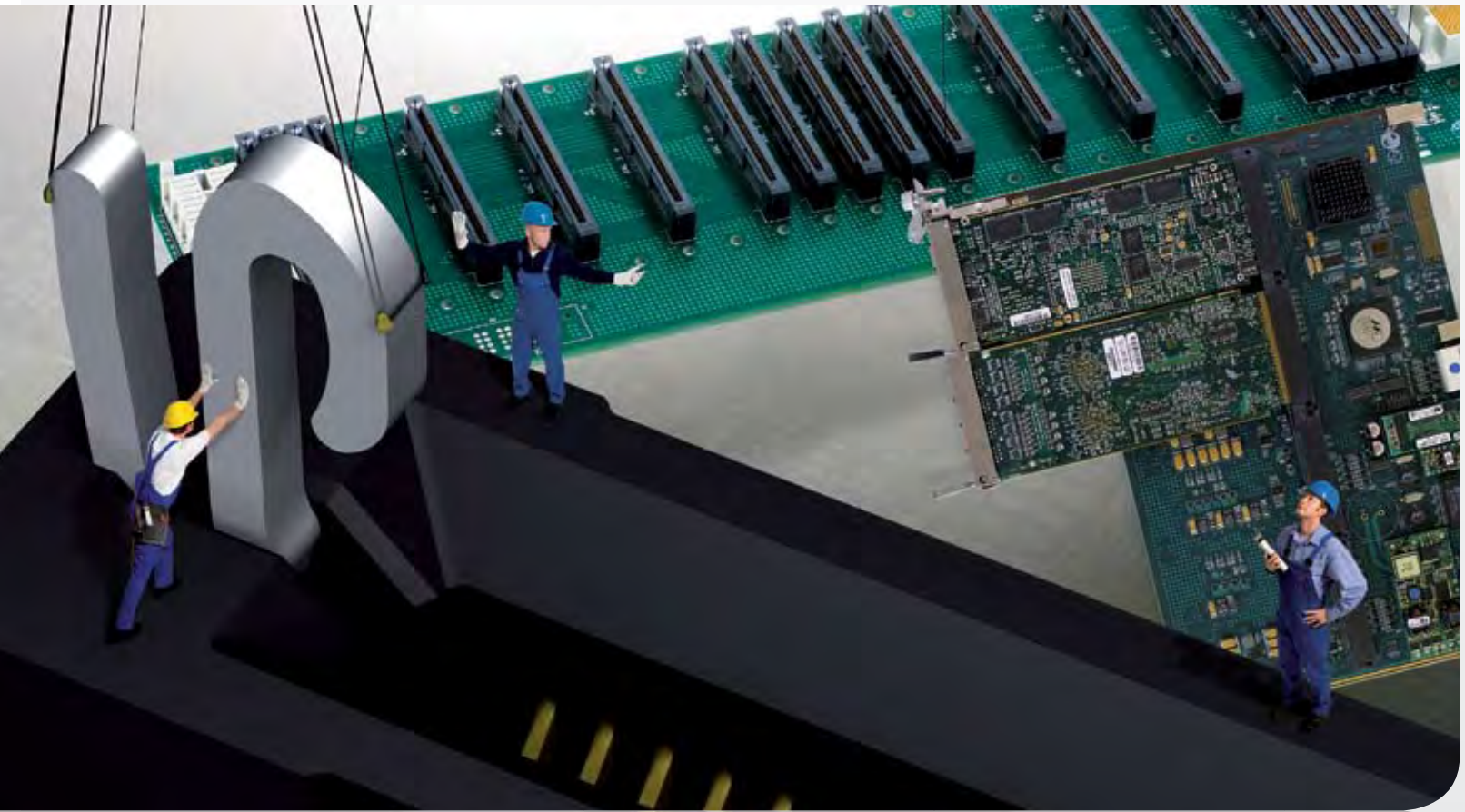
FPGAs, on the other hand, are becoming much easier to develop. New, higher-level language-based development flows, leveraging C or MATLAB for example, are enabling developers to approach FPGA development from a more familiar, abstract perspective. Advanced tools such as The Mathworks Simulink have the potential to provide a graphical-based object-oriented development environment for FPGA development as well as the development of hybrid FPGA/GPP-based systems.

Significant research is now underway in both industry and academia to find new, more effective ways of using FPGAs in embedded systems. The greater use of high-level development frameworks and systems for easily integrating processor and FPGA computing holds the promise of using FPGAs in areas traditionally reserved for general-purpose or DSP processors. A number of standards efforts such as OCP-IP (www.ocpip.org), the Spirit Consortium (http://www.spiritconsortium.org) and OpenFPGA (www.openfpga.org) are showing promise for simplifying the FPGA development and integration process.

As these tools, methodologies and frameworks continue to evolve, it is likely that in the near future FPGAs will be increasingly considered for applications that are not as SWaP-challenged as today's uses. The supercomputing community is already seeing this trend in cases where FPGAs are being used as coprocessors to GPPs. Even a 2x or 3x improvement in certain key algorithms can produce significant SWaP savings for an embedded system. As the relative pain of developing for FPGAs—long development cycles, specialized talent, and so on—continues to ease, one can expect that these smaller SWaP savings will become even more attractive to developers and users. ■■

Xilinx
San Jose, CA
(408) 559-7778.
[www.xilinx.com].

con:card+
the most reliable AdvancedMC™ connectors



AdvancedTCA® μTCA™

A new standard in reliability

con:card+ is a new quality seal that identifies connectors providing the highest level of mating reliability for AdvancedMC™ modules.

con:card+ connectors feature the unique GuideSpring technology. The GuideSpring pushes and holds the AdvancedMC™ module against the connector housing.

By systematically positioning the module precisely in the connector, **con:**card+ connectors reduce the maximum possible offset between connector contacts and module pads by 60%, thus significantly increasing the mating reliability of MicroTCA™ backplanes and AdvancedTCA® carrier blades.

By preventing module float in the connector, **con:**card+ connectors also enhance the reliability of AdvancedMC™ systems under shock and vibrations.

Learn more about the 5 **con:**card+ features at **www.concardplus.com**

innovation by

HARTING®

System Development

GPP, DSP, FPGA Trade-Offs

MPPA Strategy Puts DSP/FPGA Dominance in Check

FPGAs and DSPs have recently held the high ground in military signal processing apps. Now Massively Parallel Processor Arrays (MPPAs) are weighing in, bringing benefits not found in those other approaches.

Paul Chen, Director of Strategic Business Development
Ambric

High-performance, real-time embedded applications are characterized by complex algorithms that must process, deterministically, a large amount of data within a given time interval. Advanced military Surveillance, Intelligence and Reconnaissance (SIR) sensor packages that support multi-mode operations raise the bar even higher, not only in processing performance but also in programmability and run-time reconfigurability. A good example of this is AN/SPY-3 (Figure 1) long-range, multi-function radar. It supports theater ballistic missile defense, short- to medium-range searching and multi-target tracking.

For Electro-Optic (E-O) applications, most systems integrate multiple detectors of different spectrums in one package. The trend now is toward using the same processing subsystem to satisfy the computational needs of various modes of operation. Performance, scalability, programmability, reconfigurability and ease of development are major requirements for processing solutions to achieve this. To understand the trade-offs involved, it's useful to compare the traditional approaches to embedded systems development—Application-specific Integrated Circuit (ASIC), Digital Signal Processor (DSP) and Field-Programmable Gate Arrays (FPGAs)—with a new and innovative solution: Massively Parallel Processor Arrays (MPPAs).

Figure 1

AN/SPY-3 Multi-Function Radar (MFR) is an X-band active phased-array radar designed to meet all horizon search and fire control requirements for the 21st-century fleet. MFR is planned for introduction in CVN-77 and next-generation CVNX aircraft carriers and the DDX surface warship programs. The CVN-77 George H.W. Bush is shown here at its launch at Northrop Grumman Newport News in October 2006.

Today, ASICs, DSPs and FPGAs are commonly used by embedded applications to meet processing needs. ASICs provide excellent performance and are very power-efficient. However, they require a very high investment in NRE, require huge engineering efforts and long development times, and lack programmability. Due to low volumes, ASICs are not typically a choice for most military applications.

SOLUTIONS ARE IN SIGHT

Few industries have applications with the complexity, strict safety standards, and low error tolerance of

DEFENSE & AEROSPACE

Work with an advanced microelectronic and display partner who offers:

- Semiconductor packaging for specific circuit board density, weight and environmental requirements
- Hundreds of COTS memory devices and processors for high-reliability defense applications
- Enhanced and ruggedized LCD panels for high-performance aerospace applications
- Interface and electromechanical devices built to precise performance and design specifications
- AS/9100 certified manufacturing facilities

REVIEW OPTIONS. GET ANSWERS.

Visit **www.whiteedc.com/delivers**
or call **602.437.1520.**

WHITE ELECTRONIC DESIGNS

WWW.WHITEEDC.COM

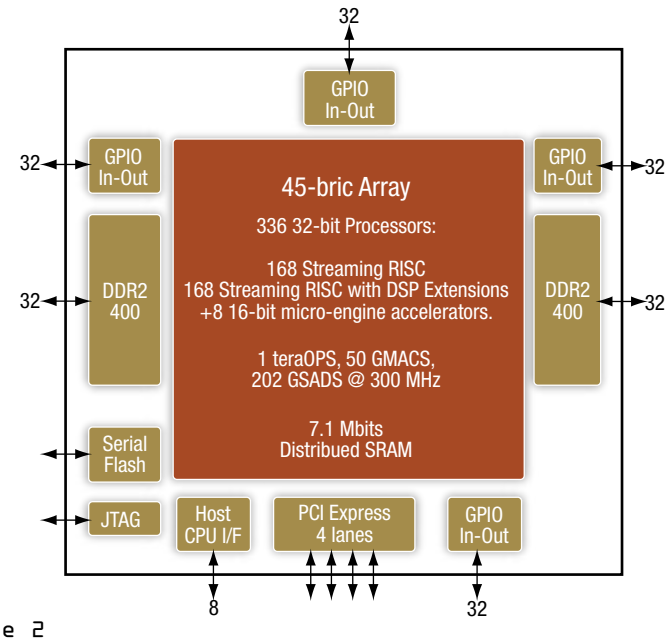


Figure 2

Ambric's Am2045 is a standard-cell 130 nanometer ASIC. Shown here are the external interfaces, including external SDRAM interfaces, a PCIe interface and four general-purpose I/O (GPIO) ports.

FPGAs are a step down from ASICs in performance and a step up in ease of use. Because they rely on reprogrammable logic, FPGAs are inherently less silicon-efficient than ASICs but offer more flexibility because they are programmable. FPGAs are programmed at the Register-Transfer-Level (RTL), applying very basic operations such as Boolean equations and control logic to registers, in languages such as Verilog or VHDL. Programmable I/O and a large number of pins make FPGAs well suited for interfacing devices.

High-end DSPs are at the opposite end of the spectrum from ASICs. DSPs are processors programmed in a mixture of a high-level language and assembly language, a trait that is appealing to software developers. Most DSPs include hardware multipliers for efficient multiply and multiply-accumulate operations. They support two memory accesses per cycle to more efficiently run algorithms such as filters, which operate on two arrays at once.

Programming complexity is a major challenge with FPGAs. Writing code for an FPGA requires two distinct sets of skills, of which few people possess both: good knowledge of hardware constraints, such as timing closure and gate-level coding, and the good software programming skills and DSP theory knowledge needed to efficiently implement complex algorithms. Another problem with FPGAs is the complexity involved in creating a correct design. FPGA designs of average complexity often take hours to place and route. This significantly impedes code development and validation. This increased programming complexity results in longer development times or in designs that do not efficiently use the available logic.

DSP Programing Advantages

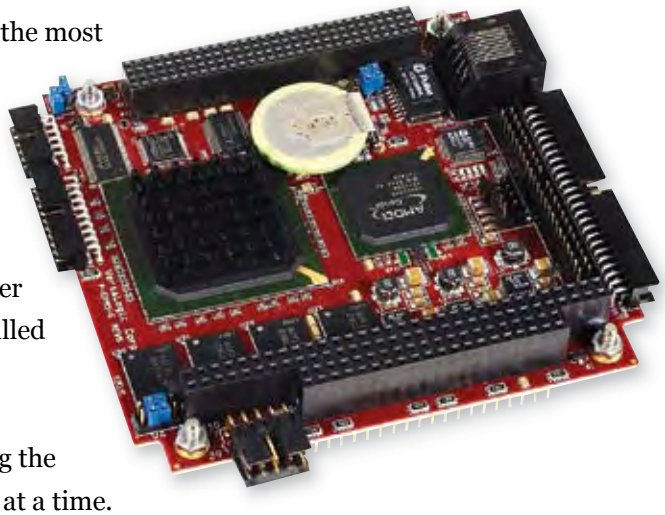
The strength of DSPs is their ease of programming: software developers code entire applications in a mix of high-level and assembly languages, a key advantage compared with using RTL. High-end DSPs have an increased pipeline and are packed with specialized hardware. This requires programmers to handcraft code, such as instruction rescheduling and loop unrolling, to use these features to achieve the desired performance.

The complexity of DSP programming has increased exponentially with the recent introduction of multicore DSPs. In these devices, several identical DSP-oriented cores are connected to share mem-

Your Products Are Expected To Protect Lives

Our products help you succeed

Protecting lives and property are at the heart of every security application. At VersaLogic our embedded computers have been designed into some of the most sophisticated and high profile security equipment being used today. And because we understand that our customer's products must meet special requirements, every board we make is run through exhaustive inspections and quality tests, ensuring that we deliver only the best. With our world class service and five year availability guarantee, things won't stall out on your production line either. Whether you need one of our standard products or a customized version, our skilled technical staff will work with you to meet your exact requirements.



Contact us to find out how for more than 30 years we've been perfecting the fine art of extra-ordinary support, and on-time delivery: One customer at a time.

1.800.824.3163
1.541.485.8575
www.VersaLogic.com/sec

VERSALOGIC CORPORATION

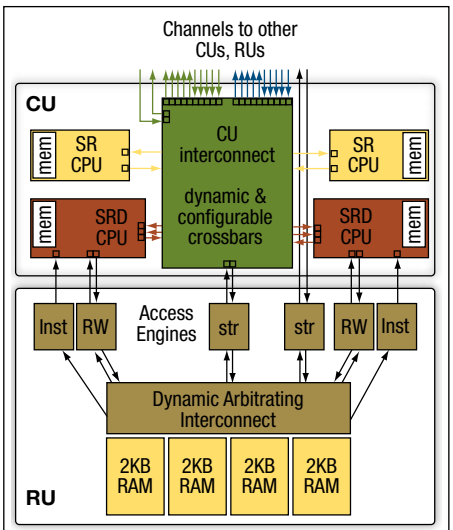


Figure 3

The core of the Am2045 is a 9-row by 5-column array of building blocks (brics). Shown here is a CU-RU pair within a bric cluster. Each bric has two Compute Unit (CU) processor clusters and two RAM Unit (RU) memory clusters. One CU contains two 32-bit streaming RISC processors (SRs) and two 32-bit streaming RISC processors with DSP extension (SRDs) for math-intensive processing and larger, more complex objects.

ories that store code and data and are used for inter-processor communication. To achieve desired performance gains, software developers face the challenges of distributing the application workload among the limited number of cores at all times and minimizing the overhead of inter-core communication. In addition, writing multi-threaded code is difficult and highly prone to errors.

Software developers must write re-entrant code, which does not scale well. Keeping multi-threaded code safe, finding enough work to run on all cores at once, and preventing memory from becoming a bottleneck becomes harder as the number of cores communicating through the same shared memory increases. As a result, the advantage of DSP programming ease quickly diminishes as DSP architectures become more complicated.

Neither FPGAs nor DSPs do well at supporting run-time dynamic reconfiguration. The best they can do is achieved by reloading the entire device or cores. The time it takes to reconfigure an FPGA and the DSP memory, plus the inflexibility of the I/O connection, makes dynamic reconfiguration problematic.

The MPAA Approach

In contrast with multicore DSPs, which have a limited number of processors (8-12), MPPAs have hundreds of processors. Each processor in an MPPA is strictly encapsulated and accesses only its own code and memory. Point-to-point communication between processors is directly realized in a configurable interconnect. Each processor runs a specific task with the guarantee that no other processor will affect its state. Hundreds of processors enable a full application to be divided naturally into a number of functions, each of which maps into a separate processor.

Implanting the code for each processor on an MPPA is usually much simpler than doing so on any high-end DSP. That is because no individual processor must be highly optimized to single-handedly meet the application requirements. For example, the Ambric Am2045 has 336 processors with more than one TeraOps of aggregate performance. Another advantage of MPPAs is the scalability of their architectures. Taking the Ambric Am2045 as an example, each block (bric) contains eight processors and local memories that are connected in a configurable point-to-point interconnect.

A global fabric connects brics together for remote communication. This approach, similar in concept to what FPGAs offer at the gate level, provides a straightforward path to producing more powerful parts with faster processors, all without complicating the system architecture. Unlike high-end DSPs, MPPAs do not need to rely on the continuous addition of new features to the processor architecture to guarantee a steady increase in performance.

Comparing MPPAs, DSPs and FPGAs

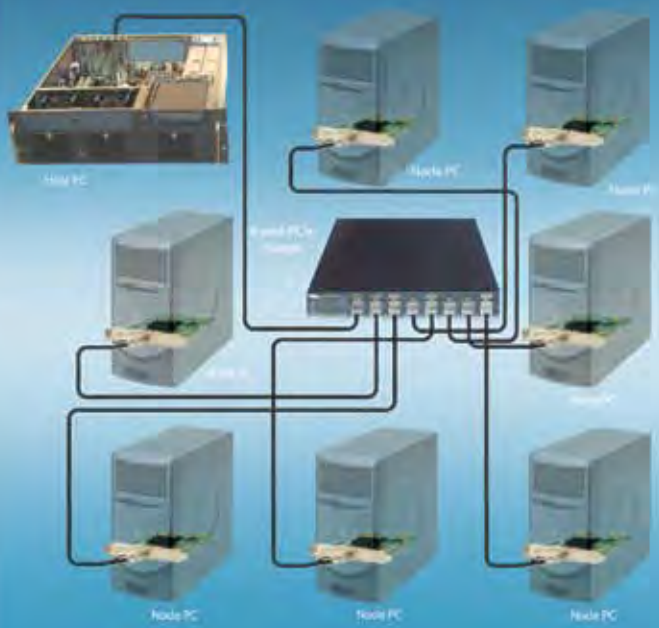
In terms of performance, MPPAs compare well with high-end DSPs and FPGAs. High-performance applications generally offer numerous opportunities for the data or functional parallelism that enables an MPPA to outperform the fastest high-end DSP by a large margin.

PCIe over Cable

I/O EXPANSION

- PCIe x1, x4 and x8 adapters
- Transfer rate up to 20Gb/s
  Gen 2 up to 80Gb/s
- Software transparent

HIGH-SPEED NETWORKING
with SuperSwitch™



- x4 at 10Gb/s
  Gen 2 up to 80Gb/s
- ExpressNet™ Software
  Direct data transfer
  TCP/IP

MAX EXPRESS™

ONE STOP SYSTEMS
2235 Enterprise, Suite 110
Escondido, CA 92029
Tel (760) 745-9883 Fax (760) 745-9824
(877) GET-CPCI
(438-2724)

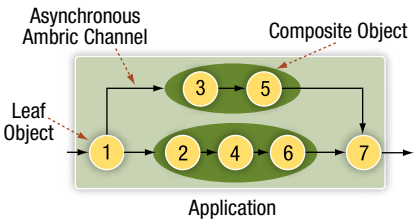


Figure 4

Programming of the Am2045 platform is made easy using the Ambric Structural Object Programming Model. Objects may be aggregated into hierarchies of composite objects and run independently at their own rates. By implementing a streaming protocol in silicon over their channels, Ambric processors run asynchronously locally, while being globally synchronized automatically, all with no need for a real-time operating system.

For example, according to several benchmarks published by Texas Instruments (TI), the Ambric Am2045 outperforms the TIC64X by 10 to 20 times.

The Am2045 is a standard-cell 130 nanometer ASIC. The core of the Am2045 is a 9-row by 5-column array of building blocks (brics) surrounded by external SDRAM interfaces, a PCIe interface, and four general-purpose I/O (GPIO) ports (Figure 2). Each bric has two Compute Unit (CU) processor clusters and two RAM Unit (RU) memory clusters (Figure 3). One CU contains two 32-bit streaming RISC processors (SRs) and two 32-bit streaming RISC processors with DSP extension (SRDs) for math-intensive processing and larger, more complex objects.

An SR holds 128 16-bit instructions. An SRD holds 256 32-bit instructions, and can fetch more instructions or data from the RU next to it. The resource (processor and memory) interconnection is made by loading their input and output channel mapping registers. The programming of the Am2045 platform is made easy using the Ambric Structural Object Programming Model (Figure 4). Objects consist of one or more software programs running concurrently on an asynchronous array of Ambric processors and memories.

Objects may be aggregated into hierarchies of composite objects and run independently at their own rates. By implementing a streaming protocol in silicon over their channels, Ambric processors run asynchronously locally, while being globally synchronized automatically, all with no need for a real-time operating system. If a producer processor executes an output instruction to a channel that is full, the processor stalls until the channel is drained. Similarly, a consumer processor is automatically suspended if, on a read instruction, a channel is empty, and automatically resumes execution once data appears in the channel.

The Ambric Integrated Design Environment (IDE) is a comprehensive software development environment based on the industry-standard Eclipse environment. With the Ambric IDE, developers can describe design structures, implement algorithms in Java or assembly language, and re-use already validated objects from the library. The functional simulator verifies a design's functional correctness and its expected execution behavior. The symbolic debugger makes multi-processor code debugging easy whether the code is running in simulation or on the device. A designer typically becomes productive after one day of training to use the tools. For example, the implementation of a 32-channel ultrasound beamforming algorithm took just two weeks.

Since the initial configuration of an Ambric MPPA is itself a configured application, reconfiguring at runtime is straightforward and fast. Because objects are independent and encapsulated, reconfiguration of one object can happen while other parts of the application continue to run normally. It took only 11 milliseconds to configure an application that nearly filled the entire Am2045 device from the DDR2-400 SDRAM interface or the four-lane PCI Express. Reconfiguring the application using a 4 Mbit, 33 MHz serial flash chip took 112 milliseconds. Another case showed that the time to reconfigure 13 percent of the Am2045 chip took fewer than six microseconds. ▮▮

Ambric
Beaverton, OR.
(503) 601-6500.
[www.ambric.com].

ACM/EDAC/IEEE 45th DESIGN AUTOMATION CONFERENCE
JUNE 8-13, 2008 • ANAHEIM, CA • WWW.DAC.COM

Where electronic design meets...

Mark your calendars for the 45th Design Automation Conference (DAC) at the Anaheim Convention Center, June 8-13, 2008, in Anaheim, California, USA.

Only DAC Offers:

- A robust technical program covering the latest research developments and trends for the design of SoCs, FPGAs, ASICs, digital ICs and more.
- Worldwide attendance from leading electronics companies and universities.
- Over 250 companies displaying electronic design technologies and services.

Highlights Include:

- Wireless Theme sessions
- Management Day on Tuesday, June 10
- Paper sessions featuring leading technical research
- New "iDesign" and WACI sessions
- Dynamic Panels Sessions
- DAC Pavilion Panels on the show floor
- 19 collocated events and workshops
- Full-day and Hands-on Tutorials
- *New! Exhibitor Forum on the show floor*

2008 Keynotes:

- **Justin R. Rattner**, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.
  EDA for Digital, Programmable, Multi-Radios
  Tuesday, June 10
- **Sanjay K. Jha,** COO and president of Qualcomm CDMA Technologies
  Challenges on Design Complexities for Advanced Wireless Silicon Systems
  Wednesday, June 11
- **Jack Little,** President, CEO, and a Co-founder of The MathWorks, Inc.
  Idea to Implementation: A Different Perspective on System Design
  Thursday, June 12

Register on or before May 19th to receive 20% off Conference Registration or for a FREE Exhibit-Pass!

REGISTER ON-LINE TODAY: www.dac.com

Sponsored by: ACM EDA CONSORTIUM IEEE

Supported by: CEDA IEEE CIRCUITS & SYSTEMS SOCIETY CANDE sigda

In Technical Cooperation with: SSCS

45 YEARS
DESIGN AUTOMATION CONFERENCE

MIL-STD-1553 Joins the Multi-Function Board Trend

Still popular as a solution for low-latency, high data integrity interface needs, 1553 has maintained its viability in a variety of military applications. Multi-function board solutions that include 1553 are strengthening that legacy.

Jeff Child,
Editor-in-Chief

While still an avionics bus at heart, the MIL-STD-1553 bus continues to play a role in a wide variety of systems such as tanks, ships, missiles and satellites. The B-2 Spirit Bomber's (Figure 1) avionics systems are the heart of the stealth bomber's combat capability, linked together through a 1553 network. Even the International Space Station makes use of 1553.

Despite its three decades of age, this venerable interface technology remains the dominant, internationally accepted data bus standard for many military platforms. And for applications where data integrity and low latency are the priorities, MIL-STD-1553 is likely to remain the military interface of choice. Meanwhile Fibre Channel, Ethernet and Extended 1553 (E1553) top the list of possible upward migration paths from 1553.

Last summer, Edgewater Computer Systems' Extended 1553 data bus technology successfully completed a flight test on board a U.S. Air Force F-16 in Tucson, AZ. The primary purpose of the test was to demonstrate an increase in network capacity roughly 100 times the legacy throughput with no interference to the legacy 1553 system. During the flight test, the ANG Block 30 F-16 performed typical mission flight and aircraft maneuvers including multiple-target tracking with radar and sensor systems and high-G turns. Extended 1553 operated concurrently with the legacy 1553 operation. This flight test is a significant milestone for the E1553 project, and solidifies that the technology is at an advanced technical readiness level in support of operational flight.

Fueling 1553's acceptance is its rich ecosystem of product form factors. As the Product Roundup on the following pages shows, products with 1553 interfaces exist in myriad board form factors including VME, CompactPCI, PMC, PrPMC, PC/104 and others. Within that scope, a trend has been gathering momentum whereby one or more 1553 channels are becoming part of multi-function board-level solutions. Thanks to the magic of today's level of semiconductor integration, a new generation of multi-function mezzanine products has emerged. These enable military system designers to blend a variety of I/O functions onto a single PMC or similar form factor. Multi-function solutions available are combining 1553 with everything from ARINC-429 to RS-232/422/485 and even IRIG-106 Recording. ▮▮

Figure 1

The avionics systems of the B-2 Spirit Bomber are linked together through a 1553 network. Shown here is a B-2 Spirit Bomber being refueled by KC-135 from the 927th Air Refueling Wing, Selfridge ANG Base, Michigan, as it returns from Scott Air Force Base, Illinois during a civic leader tour.

Data Bus Products...

Innovative & Enduring

Mil-Std 1553 Components

Data Bus Products
Manufacturers of High Quality, Innovative Avionics

Mil-Std-1553 Couplers: (1) through (16) stub ports • Terminators: Versatile configurations and values
Connectors / Adapters / Transition Hardware • Multiple Bus / Stub Switches and Relays
Bus and Stub Cable Assemblies: Always from stock • Custom Parts
All Products Manufactured in The U.S.A.

DATA BUS PRODUCTS

Phone: 516-365-8464
Fax: 516-365-3946
www.databusproducts.com

Technology Focus:

1553 Boards Roundup

cPCI Card Aims at 1553 Test and Measurement

1553 has found its way onto just about every major embedded board form factor used in the military and avionics applications. For it part, AIM GmbH has introduced its fourth generation, advanced cPCI (6U), ACX1553-2/4/8 card for analyzing, simulating, monitoring and testing of up to eight MIL-STD-1553 data buses, which provide the

inter-connection of the onboard sub-systems. The card is available with two, four or eight Dual Redundant MIL-STD-1553 streams on one single cPCI (6U) card. Full protocol testing and simulation of the Bus Controller, Multiple Remote Terminals and Chronological Monitoring is possible on all buses at full bus rates.

The ACX1553-x incorporates 2 or 4 high-performance 400 MHz Xscale Processors and an additional 400 MHz Intel IOP Application Support Processor. It is equipped with 4/8 Mbytes Global memory expandable up to 16/32 Mbytes plus 128 Mbyte ASP memory. An onboard IRIG-B time Encoder/Decoder unit provides a sinusoidal output and free wheeling mode for time tag synchronization on the system level. The ACX1553-2/4-DS version, available as an option and known as MILScope, also incorporates an onboard A/D converter on the first channel to provide the measurement, test and verification of the MIL-STD-1553 waveform and detect faulty bus conditions without the need of an external oscilloscope.

AIM-USA
Elkhorn, NE.
(866) AIM-1553.
[www.aim-online.com].

Multi-Function PMC Does 1553 and More

The magic of today's level of semiconductor integration has enabled the emergence of multi-function mezzanine products. These allow military system designers to blend a variety of I/O functions onto a single PMC. With just that in mind, Aitech Defense Systems now offers a compact, multi-I/O PMC that provides a variety of configuration options for the highest levels of flexibility in different I/O environments. The low-power, single-width M705 features an unprecedented level of PMC density with up to five dual-channel, dual-redundant MIL-STD-1553B channels, 16 ARINC-429 receive channels and eight ARINC-429 transmit channels, up to six RS-232/422/485 serial channels and eight opto-isolated digital discrete input channels, all of which reduce the number of I/O cards required when developing subsystems. Additional board options include an ARINC 708 Weather Radar interface contained as VHDL within the large on-board FPGA.

The MIL-STD-1553 (STANAG 3838) channels support BC/RT/MT operation modes and offer 128K bytes (64K words) of dual-port RAM per channel. The discrete input channels serve as general-purpose I/O ports that connect to the GPIO FPGA, but are primarily used to externally assign the RT address to the MIL-STD-1553 channels. The PMC is available in the widest temperature range of -55°C to +85°C (-67°F to +185°F) and with software in rugged and military levels of ruggedization. Pricing for the M705 starts at $3,650.

Aitech Defense Systems
Chatsworth, CA.
(888) 248-3248.
[www.rugged.com].

1553 PMC Boasts Auto Message Transfers

Efficient message handling is a helpful feature in 1553 subsystems. Along those lines, Alphi Technology offers the PMC-1553-PLX, a single-wide PMC form factor, which is based on the UTMC SUMMIT chip. Providing one or two dual redundant

channels, the card provides system designers a versatile solution to multiplexed serial data bus design requirements. The PMC-1553-PLX board minimizes PMC host overhead with its automatic execution of message transfers, interrupt handling and generation of status information. In the Bus Controller mode, the PMC-1553-PLX implements a linked list message scheme to provide the system with message chaining capability. In the Remote Terminal mode, time tagging and message history functions are available. The PMC-1553-PLX also allows multiple message processing, programmable automatic message delay, and automatic polling and retry.

Standard operating temperature for the board is 0 to +70°C, with an optional temperature range of -25° to +80°C. The board's humidity range is 5 to 90 percent and it operates at altitudes from 0 to 10,000 feet. Power consumption is 1.5W. Shock and vibration specs for the product are 0.5G RMS, 20-2000 Hz rand and 20G, 11 ms, 0.5 sine. Mean time before failure is rated at 250,000 hours. Software support for the two products include a "C" Library Toolkit and driver support for many of the real-time OSs, such as Windows, NT, VxWorks and OS-9.

Alphi Technology
Tempe, AZ.
(480) 838-2428.
[www.alphitech.com].

1553 BOARDS SHOWCASE

Featuring the latest in 1553 Boards technology

C108 Single Board Computer

- Upgraded high performance, rugged 6U VME SBC
- New and legacy military embedded applications
- Includes 8 GB USB SSD for onboard file storage
- 1.4 GHz of processing power via the PowerPC MPC7448 processor
- Reduced heat generation and increased reliability3
- Two dual-redundant MIL-STD-1553B interfaces

Aitech Defense Systems, Inc.
Phone: (888) 248-3248
Fax: (818) 718-9787
E-mail: sales@rugged.com
Web: www.rugged.com

MIL-Std

- **Connect your hardware to your favorite Avionics**
- IP-1553 is a MIL-STD-1553 compatible interface
- Dual redundant BC/RT and Monitor capabilities
- 64K of RAM per channel
- Programmable master, target and monitor operation
- Direct coupled and Transformer coupled operations
- 8/32 MHz. IP Bus compatible
- Micro-ACE 1553 interface support via IO/INT/Memory spaces

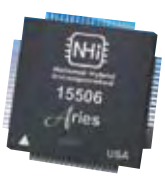
Dynamic Engineering
Phone: (831) 457-8891
Fax: (831) 457-4793
E-mail: sales@dyneng.com
Web: www.dyneng.com

Cable Harnesses and Custom Assemblies

- In-house, highly skilled technicians
- High-volume production to low-volume custom
- Large connector and cable inventory
- CAD Design Capability
- Detailed Drawing Proofs
- Prototype Development
- Testing
- Build to Print
- On-time delivery

MilesTek
Phone: (866) 524-1553
Fax: (940) 591-7086
E-mail: salesinfo@milestek.com
Web: www.milestek1553.com

The AriesTMSeries (Advanced Replacement Interface Engine Solution)



- Fully Integrated MIL-STD-1553 A/B STANAG 3838 Compliant Terminals
- 5 Volt Only Operation
- 4K x 16 or 64K x 16 Shared RAM
- Form Fit and Function Replacement for DDC's Mini-ACE®
- Hardware and Software Compatible with BU-61580 ACE®Series
- Flexible Processor/Memory Interface
- Cost Effective Solution

National Hybrid Inc. An Division of API Nanotronics
Phone: (631) 981-2400
Fax: (631) 981-2445
E-mail: sales@nationalhybrid.com
Web: www.nationalhybrid.com

7mm Dual 1553 Data Bus Transceivers

- +3.3V or +5V Versions
- Smallest Available Mil-Std-1553 A&B, Mil-Std-1760 Dual Transceivers
- Dimensions: 7mm x 7mm x 2mm
- Single supply 5V or 3.3V
- 1.5 Watts Max Power Dissipation
- Output driver Withstands Short Circuit Fault
- Proprietary Monolithic Design Provides Outstanding Thermal Impedance Characteristics
- Designed to Replace Holt HI-1565/1566 Devices

National Hybrid Inc. An Division of API Nanotronics
Phone: (631) 981-2400
Fax: (631) 981-2445
E-mail: sales@nationalhybrid.com
Web: www.nationalhybrid.com

Ruggedized PC/104 Avionics Network Gateway

- Built-In Networking
- Pre-Integrated and Ready-To-Run Configurations
- Extended Temperature, Vibration, and Shock
- Mix-And-Match from a Wide Selection of I/O Interfaces
- Real-Time Low Latency Operation System
- IRIG-B Precision Time Reference
- Data Recording Option

NetAcquire Corporation
Phone: (888) 675-1122
Fax: (888) 670-1122
E-mail: info@netacquire.com
Web: www.netacquire.com

PrPMC Board Marries 1553 and PowerPC CPU

The PMC is probably the most common platform for 1553. But Ballard Technology puts a twist on that with its latest MIL-STD-1553 offering that lets users decide on one or two dual redundant 1553 interfaces and then use the PowerPC function to handle responses, interact with other cards or just have the PrPMC as back-up. The new Ballard OmniBus PMC card offers a rugged, conduction-cooled solution for MIL-STD-1553 applications. Ballard's PMC card is available in commercial or conduction-cooled versions and offers users a monarch/non-monarch PrPMC with DMA and 1 or 2

dual redundant 1553 interfaces at an affordable cost.

The OmniBus 1553 PMC can be used as a peripheral to a host processor system, or it can operate as a stand-alone device utilizing the PowerPC embedded processor. The MIL-STD-1553 channels are implemented as hardware modules external to the processor. This results in the user having full utilization of the processor while protocol operations are autonomously performed in hardware. The OmniBus architecture ensures all schedules will be maintained and all data will be received on fully loaded 1553 databuses.

Ballard Technology
Everett, WA.
(425) 339-0281.
[www.ballardtech.com].

Switch Panel Multiplexes Sixteen 1553 Buses

When implementing avionics simulations or test scenarios, the chore of rewiring between different 1553 bus channels can be time-consuming. Addressing that problem, Curtiss-Wright provides the MBX1553 Multiplex Bus Switch. The switch is designed to enhance virtually any MIL-STD-1553 system by providing a "virtual patch panel" housed in a 19-inch rack-mountable 1U chassis. This 16x16 crosspoint switch provides differential connections from 16 transformer-coupled Line Replaceable Unit (LRU) ports to 16 MIL-STD-1553 differential buses. The LRU units can be any MIL-STD1553 device: bus controller (BC), remote terminal (RT), or bus monitor (BM). Although the switch supports 16 non-redundant LRUs, it can also be used with dual (or more) redundant devices.

The MBX1553 switch provides 16 LRU ports via standard concentric twinax connectors on the front of the unit. The 16 bus port connections, which all use the same type of connectors, are available on the rear of the unit. Multiple switches may also be connected together if more LRU inputs or bus connections are desired. The MBX1553 switch configuration is controlled via an internal processor and associated RS-232 serial port. LRU ports may be selectively connected to (or disconnected from) a specified bus. The internal controller ensures that each LRU is not simultaneously connected to more than one bus. The MBX

switch command set is thoroughly documented in the user's guide, allowing the user to provide control through a dumb terminal or to write separate communication software.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

PMC Blends 1553 and IRIG-106 Recording

Multi-function cards are the wave of the future for military I/O boards. The IRIG-106 timing standard is a natural function to combine with 1553. Doing just that, Data Device Corporation (DDC) has introduced a new MIL-STD-1553 PMC board (BU-65578F/Mx) that provides up to eight dual redundant MIL-STD-1553 channels, eight user-programmable Digital Discrete I/Os, eight user-programmable Avionics level (+35V) Discrete I/Os, an IRIG-B time synchronization

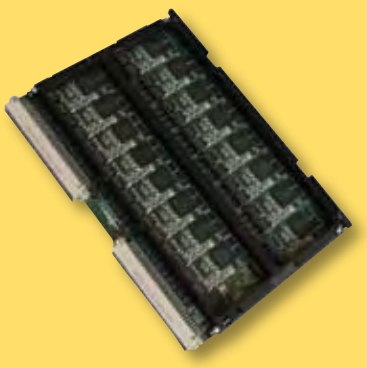
input, and an IRIG-B time generator. The card can be ordered with either rear or front panel I/O and is available for convection- or conduction-cooled applications.

DDC's new Extended Enhanced Mini-ACE (E²MA) Architecture is utilized for the 1553 interface. An evolution of DDC's field-proven, industry-standard Enhanced Mini-ACE Architecture, the new E²MA architecture builds upon previous generations of DDC products while maintaining full API compatibility. Each 1553 channel supports new standard features such as 1 Mbyte RAM with parity per channel, 48-bit/1µs or 100 nS time tag and built-in self-test. An intelligent hardware offload engine provides extremely low PCI bus and host CPU utilization while storing 1553 Monitor data in a convenient IRIG-106 Chapter 10 format. The industry-standard IRIG-106 Chapter 10 format is commonly used for digital flight data recorders.

Data Device Corp.
Bohemia, NY.
(631) 567-5600.
[www.ddc-web.com].

Multi-Function VME Card Is Conduction-Cooled

High channel count, onboard self test and loop back all rank high on the list of priorities when choosing a 1553 solution. Excalibur Systems addresses all those points with its latest card in its MIL-STD-1553 Px family. The EXC-1553ccVME/Px is a multi-channel (up to sixteen) MIL-STD-1553A/B interface board for conduction-cooled VME systems. The channels are fully independent, dual redundant, each of which can operate simultaneously as a Bus Controller and up to 32 Remote Terminals, and also as a Triggerable Monitor. The card supports extensive error injection and detection capabilities, and an internal loop back, which requires no external cabling.



The card has an operating temperature range of -40° to +85°C and may optionally be ordered with conformal coating. It is supplied with C drivers, including source code and Merlin+ Windows software. The EXC-1553ccVME/Px is designed for rugged embedded applications, especially those requiring operation in a sealed, conduction-cooled, extended temperature environment.

Excalibur Systems
Elmont, NY.
(800) MIL-1553.
[www.mil-1553.com].

10 Mbit/s MIL-STD-1553 Rides PMC

The 10 Mbit/s flavor of MIL-STD-1553 boosts the venerable 1553 protocol up by an order of magnitude of bandwidth. The P-10SF from GE Fanuc Intelligent Platforms offers one or two channels of dual-redundant 10 Mbit 1553 Notice 2 protocol using RS-485 transceivers. This interface is an excellent choice for flight controls, actuators, electro-pneumatic controllers or for similar applications of standard 1553 requiring higher data rates. The P-10SF is available as a native PMC interface or in PCI or CompactPCI

formats (supplied on carrier boards). Each P-10SF PMC interface may be obtained in one or two dual-redundant channels on a PCI and cPCI carrier with front bezel or P14 (rear) I/O and optionally in ruggedized, extended operating or conduction-cooled temperature configurations.

Each interface provides BC, single RT or BM functionality with a portable, high-level API software that includes driver support for Windows and VxWorks (PPC) to reduce application development time. Standard features include -20V to 25V Common Mode Voltage Range, Bus I/O Protection to over 16-kV HBM, Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions, and greater than 100 mV Receiver Hysteresis for the RS-485 transceivers. It also includes 48-bit message time tagging, extensive BC and RT link-list structures, error detection, advanced BC functionality, automatic / manual RT Status Bit and Mode Code responses, along with Post, PBIT, IBIT (Built-in Tests) and cable wrap testing.

GE Fanuc Intelligent Platforms
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

PMC Marries ARINC 429, 1553, General-Purpose I/O

Some avionics communications modules provide MIL-STD-1553, while others offer ARINC 429. The PMC-6L is an avionics communications card from Thales Computers—a subsidiary of Kontron—that offers both in a single card. The PMC-6L combines ARINC 429 channels (two transmit and four receive), a single redundant MIL-STD-1553 channel, up to six serial channels and up to 16 general-purpose I/O lines on a single standard rugged PCI Mezzanine Card (PMC). The PMC features a PCI bus (32-bit/33 MHz with 3.3V signaling, 5V tolerant) and includes a large 256K x 32-bit shared memory for I/O data buffering. The PMC-6L is available in a commercial model, a rugged air-cooled version (-40° to +75°C) or rugged conduction-cooled version (-40° to +85°C).

Every port of the ARINC 429 can be clocked at either 12.5 KHz or 100 KHz. The

dual redundant MIL-STD-1553B port can be configured either in Bus Controller or Remote Terminal mode. The serial line controller of the PMC-6L is able to manage up to six serial asynchronous or synchronous lines featuring either an EIA-485 or EIA-232 electrical interface and up to 16 general-purpose I/O (GPIO), depending on the manufacturing configuration. Support is provided for VxWorks 5.5 for Tornado 2.2. Thales' airborne systems have already started to use this mezzanine card in their operational programs. Single unit pricing of the full-featured PMC-6L ranges from $3,990 to $4,390, depending on the ruggedization level.

Thales Computers
Edison, NJ.
(732) 494-1010.
[www.thalescomputers.com].

COTS Products

Note from the Editors: In the January issue of COTS Journal *we published a Tech Focus section on Conduction-Cooled cPCI Boards. In the product roundup portion of that section we neglected to include the following product from Dynatem. We apologize to Dynatem, and to you our readers for the oversight.*

3U cPCI Card Offered in Air- or Conduction-Cooled Versions

CompactPCI, particularly in its 3U flavor, has become entrenched as a trusted solution in a wide range of military applications. Dynatem offers an Intel Pentium M-based 3U cPCI solution, available in air-cooled and conduction-cooled versions. The air-cooled C3PM (shown) supports an x86 processor that is ideal for embedded, rugged applications with its low power consumption. The high-speed 855GME & 6300ESB chipset supports a 66 MHZ PCI-X expansion bus that can fully utilize the two Gbit Ethernet ports available on the C3PM with no data transfer bottleneck. An attached sub-module supports CompactFlash for single-slot booting. I/O routed to the backplane includes a Serial ATA port, two Gbit Ethernet ports, SVGA, two USB 2.0 ports and two COM ports.

The C3RM was designed in compliance with VITA 30.1-2002 so it comes with top and bottom cooling plates that are bonded to the major components through thermal conduction and to the heat conducting printed circuit board mechanically. Wedge locks secure the C3RM in the chassis and bring the module's heat from the cooling plates and the PCB and, ultimately, the components to a heat plate in the chassis. The C3PM has no socketed components, other than the optional CompactFlash drive (PXE is supported for diskless booting), so it remains rugged in high shock and vibration environments.

Dynatem, Mission Viejo, CA. (949) 855-3235. [www.dynatem.com].

DSP/FPGA-Based VXS Card Is Conduction Cooled

VXS has found a solid niche as a "here and now" solution for marrying switched fabric performance with legacy VME backward compatibility. BittWare's latest VXS offering is the GT-6U-VME (GTV6), which features two Altera Stratix II GX FPGAs (2SGX90 or 130), two processing clusters consisting of two ADSP-TS201S TigerSHARC DSPs from Analog Devices, and up to 3 Gbytes of DDR2 SDRAM memory. This conduction-cooled board is optimized for high-end, multiprocessing applications, while also providing complete flexibility for future adaptability, ideal for existing and future military applications requiring embedded signal processing in a VXS/VITA 41 form factor.

The GTV6 implements a dual BittWare ATLANTiS framework to interface between the FPGAs and DSPs. The GTV6 also features two clusters of two ADSP-TS201S TigerSHARC DSPs, which are interconnected by a 64-bit cluster bus running at 83.3 MHz. The commercial (air-cooled) version will begin shipping Q208; the ruggedized version will begin shipping Q308.

BittWare, Concord, NH. (603) 226-0404. [www.bittware.com].

1U Microchassis Aims at Rugged Apps

The 1U "pizzabox-style" form factor is quickly gaining popularity in a host of military applications. Triple E's rugged 1U microchassis addresses inherent problems associated with electronic systems configured for military, aerospace and other harsh environment applications. The microchassis meets IEEE1101.10 and IEEE1101.11 mechanical requirements. Configured with VME64X, cPCI or PICMG 2.16 backplane, the unit allows for up to two 6U x 1.6 mm x 160 mm size boards in front, and two 6U X 1.6 mm x 80 mm direct plug-in rear transition boards. Weighing 10.75 lbs., the unit measures 19-in. rack mount (L-R) x 1.73-inches high x 11.25-inches deep. Construction features 0.036-inch thick zinc plated steel for structural integrity, durable powder coat finish and removable side walls for easy maintenance.

Unlike units with plastic card guides, this design features a patented all-extruded aluminum 901 Series card guide cluster providing exceptional stability to protect boards from vibration damage and maximum cooling airflow between slots to guard against heat buildup. The unit complies with UL, EN and CE safety specifications, and conducted and radiated EN Class B and EN ratings. Costs for units configured with cPCI backplane start at $1,650.

Triple E, Lowell, MA. (978) 453-0600. [www.TripleEase.com].

RF Power Transistor Design Targets Radar/Avionics

For a long time, advances in RF power transistor technology have been mostly incremental and evolutionary. Setting out to buck that trend, startup HVVi Semiconductors has announced what it claims is the first major advance in silicon RF power transistor design in more than 15 years. Based on the world's first High Frequency, High Voltage Vertical Field Effect Transistor (HVVFET), HVVi's new architecture delivers frequency bandwidth, voltage and power levels to radar and avionic applications that far exceed the capabilities of current bipolar and LDMOS technologies.

As part of its initial announcement, HVVi is also introducing its first three products based on this innovative new HVVFET architecture. Targeted at high power, pulsed RF applications in the L-band such as IFF, TCAS, TACAN and Mode-S, the three new devices leverage the inherent benefits of the HVVFET process to deliver high output power and high gain in an extremely compact package. All three transistors are designed to operate at 48V. The three products are targeted at commercial and military avionics and ground-based radar systems. All products operate over a wide range of supply voltages from 24V up to 48V. Evaluation kits and small quantities of the PVV1214-25, PVV1214-100 and PVV1011-300 are available now, with volume production in 3Q08. HVVi Semiconductors, Phoenix, AZ. (480) 776-3800. [www.hvvi.com].

Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected

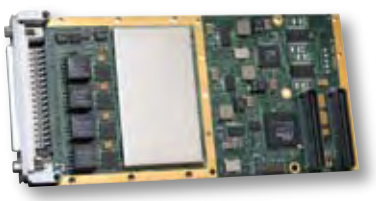
Stepper Drive Eliminates Need for DC Supply

Advances in motion control are enabling some pretty significant levels of subsystem integration in military systems—particularly in the robotics segment of the military market. Copley Controls has a panel mounting drive product called StepNet AC that runs directly on 115/240 AC at 7A peak current eliminating a separate DC supply. Pivotal benefits include servo mode operation for smooth, quiet stepper motor operation and freedom from lost steps. A range of sophisticated motion control modes are built-in: indexing, PVT trajectory tracking, camming and electronic gearing. The drive can operate stand-alone or be part of a distributed control network.

StepNet AC drives incorporate Command, Encoder and Communications interfaces that allow users to apply the single model to a wide range of stand-alone and networked architectures and applications. Actual interfaces include CAN/open, DeviceNet, ASC11/Discrete I/O, Stepper commands, ±10V position/velocity/torque command and PWM velocity/torque command. StepNet AC's "one-drive-fits-all" versatility cuts inventory costs and simplifies user logistics. Measuring 146 x 119 x 55 mm, StepNet AC drives may be mounted flat or sideways.

Copley Controls, Canton, MA. (781) 828-8090. [www.copleycontrols.com].

Development Kit Aids Multi-I/O Avionics Designs



The Multi-Function I/O subsystem trend has hit squarely into the thick of the military design world. Data Device Corp. (DDC) has introduced newly enhanced Software Development Kits (SDK) for MIL-STD-1553 and ARINC 429 data bus applications. The SDKs allow users to develop "C" source code to simulate, monitor, or troubleshoot 1553 and/or 429 data buses simultaneously or independently with support for the latest operating system versions including VxWorks 6, Linux 2.6 and Windows 2000/XP. These SDKs enable users to quickly integrate DDC's multi-protocol avionics PMC (BU-65590F/M) into their "C" code applications. A common SDK exists across all operating systems allowing the programmer portability across multiple platforms. The easy-to-use high-level functions abstract all low-level hardware accesses and memory allocation such that specific hardware knowledge is not required.

The BU-65590F/M is a multi-protocol PMC card that provides up to four dual-redundant MIL-STD-1553 channels, sixteen ARINC 429 receive channels, six ARINC 429 transmit channels, six user programmable Digital Discrete I/Os, two RS-232 Serial I/O channels, two RS-422/485 Serial I/O channels and an IRIG-B time synchronization input. The card can be ordered with either rear or front panel I/O and is available for convection- or conduction-cooled applications.

Data Device Corporation, Bohemia, NY. (631) 567-5600. [www.ddc-web.com].

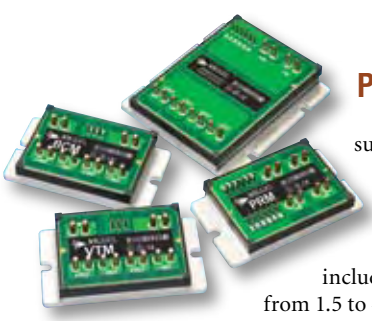
FPGA Devices Embed PowerPC and DSP

At one time military "system design" meant boards and boxes. Now complete systems can be crammed into a single FPGA device. Exemplifying that trend, Xilinx has announced the availability of its Virtex-5 FXT devices, the industry's first FPGAs with embedded PowerPC 440 processor blocks, high-speed RocketIO GTX transceivers and dedicated XtremeDSP processing capabilities.

The innovative Virtex-5 FXT platform offers the first FPGAs to provide up to two industry-standard PowerPC 440 processor blocks. Each processor, with integrated 32KB instruction and 32KB data caches, delivers up to 1,100 DMIPS at 550 MHz. Tightly coupled to the PowerPC440 blocks is a new integrated 5x2 cross bar processor interconnect architecture that provides simultaneous access to I/O and memory.

The device includes dedicated master and slave processor local bus interfaces, four DMA ports with separate transmit and receive channels, and a dedicated memory bus interface enabling high-performance, low-latency point-to-point connectivity. Virtex-5 FXT FPGA samples are now shipping for the FX30T and FX70T devices. The remaining FX100T, FX130T and FX200T devices will be available over the next six months with the first production devices scheduled to be made available in the third quarter of 2008. The FX30T device will list for $159 in 1,000-unit volumes by the second half of 2009.

Xilinx, San Jose, CA. (408) 559-7778. [www.xilinx.com].



Power Modules Boast Densities up to 390 W/in³

More efficiency and more flexibility: those are the watchwords when it comes to robust military power supply subsystems. Feeding those desires, the Brick Business Unit of Vicor introduced an advanced modular power platform: the VI BRICK. The VI BRICK family incorporates the superior technical attributes of VI Chip technology and a robust packaging that facilitates thermal management and through-hole assembly. VI BRICK BCMs provide a highly efficient solution for Intermediate Bus Architecture or point-of-load (POL) designs that require multiple output voltages. They are available with nominal input voltages including 48 VDC (11 models) and high voltage up to 380 VDC (three models) and a wide array of output voltages from 1.5 to 48 VDC. The efficiency and compact size of these modules yields power density up to 390 W/in³.

VI BRICK models are available in a base temperature grade of -40° to +100°C, operating, and -40° to +125°C, storage, with a slotted-flange baseplate and through-hole pin style. All modules of the VI BRICK family are RoHS-compliant and compatible with lead-free wave soldering processes. Pricing for modules of the VI BRICK family ranges from as low as $33 in OEM quantities.

Vicor, Andover, MA. (978) 749-8359. [www.vicorpower.com].

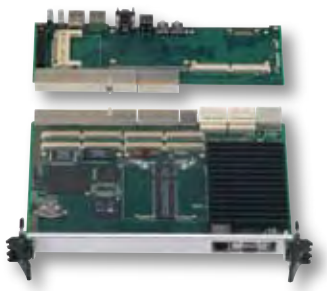
Load Sharing Module Eases Power Design

Getting the right distributed power architecture for a military system is part art, part science. Easing the way, Calex offers its Load Share Series of modules, which provide a unique "plug and play" solution for paralleling multiple DC/DC converters. Calex is the first to offer a truly modular solution significantly simplifying the task of paralleling DC/DC converters for increased current capability and/or power system redundant load sharing. No external circuitry is required with any of the Calex Load Share models. There are six models in the Series covering 3.3 to 48 volt nominal input voltages. Maximum output current is 60A. All models achieve 99 percent efficiency typically and utilize aluminium substrate technology for thermal management.

The Load Share Series utilizes "active load sharing" with low-side sensing resulting in very accurate load sharing with minimal load regulation issues. The low-side sensing in combination with the differential load share bus communication technology designed into the Load Share module results in a very high level of noise immunity. The Load Share models are housed in a 1/4 brick package measuring 2.28 x 1.45 x 0.50 inches. The baseplate operating temperature is -40° to 100°C.

Calex, Concord, CA. (925) 687-4411. [www.calex.com].

Core Duo CPU Rides 6U CompactPCI Express

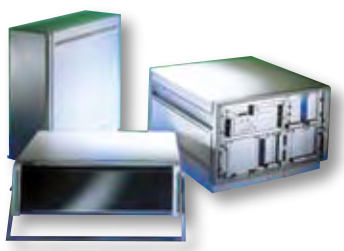


CompactPCI Express marries the tried and true cPCI form factor with the performance of PCI Express. Dynatem's latest CompactPCI Express solution is the EPD, a 6U single-slot Compact PCI Express platform based on the Intel low-power Core-Duo (Yonah) processor. CompactPCIe utilizes many of the same features as legacy CompactPCI, but changes the PCI bus for the new PCIe bus. CompactPCIe replaces the P1 and P2 connectors used in CompactPCI with new connectors that occupy the same physical area. These new connectors provide more power connections, high-speed differential pairs and a path for hybrid slots, which can hold either legacy CompactPCI or the new CompactPCIe I/O boards.

The EPD also provides full support for PICMG 2.16. Backplane PCI Express bus connections via ADF connectors XJ2 and XJ3 support either two x8 connections in two-link configuration or four x4 connections in four-link configuration. Two PMC sites are provided with 64-bit/66 MHz PCI-X routed to both sites. One of the two PMC sites also supports XMC modules with x4 PCI Express. Both sites have rear I/O accessibility. Two SO-CDIMM sockets support a total of 1, 2, or 4 Gbytes of ECC DDR-2 533 MHz memory. Retention clips provide some vibration immunity. Pricing for the EPD starts at $4,298 in single quantity.

Dynatem, Mission Viejo, CA. (949) 855-3235. [www.dynatem.com].

19-Inch Enclosures Feature Thermal Management



As processors get ever more powerful, power dissipation in the form of heat becomes a real challenge. Addressing that issue, a series of 19-inch and half-width desktop cases, 19-inch vertical and horizontal caseframes from Verotec offer outstanding versatility and thermal management. Available in 3U, 4U, 6U and 9U heights and depths of 322, 422, 522 and 622 mm, the Diplomat series of cases are equally suitable for use during system development and as a housing for production status units. The caseframes provides direct mounting for Eurocard format PCBs in an easily configurable subrack system; the cases accept any standard 19-inch component. With power densities steadily increasing, effective ventilation is of paramount importance.

All horizontal versions can be fitted with an optional 38 mm deep filtered ventilation plinth that replaces the standard base cover, allowing cool air to be drawn into the unit from below. The ventilation plinth increases air throughput and provides a uniform airflow across the full width of the unit. The cool air is drawn into the unit through a removable filter in the plinth, and is then directed through the active board area by a rear duct plate that blanks off the space behind circuit boards.

Verotec, Eastleigh, Hampshire, U.K. + 44 (0)2380 246900. [www.verotec.co.uk].

Battlefield PDA Validated for Windows Mobile 6

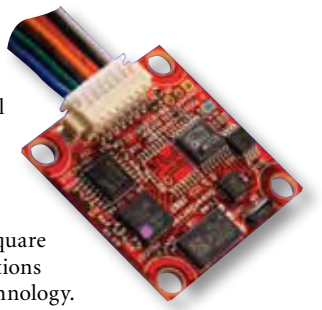
Portable, heldhand devices have become a fixture in today's military operations. Elbit Systems of America C4I Solutions Business Unit has successfully completed extensive validation testing of Microsoft Windows Mobile 6.0 on their enhanced Rugged Personal Digital Assistant (RPDA-57). The new version is C4I Solutions' fifth-generation tactical handheld computer.

The new configuration includes 128 Mbytes of RAM, 128 Mbytes of ROM and the Intel PXA 270 Processor, sporting a 524 MHz processor. What makes the RPDA-57 unique is its modular design. Customers can select various configurations for use in their applications by simply changing the expansion back on the units. From basic functionality to the U.S. Military's SAASM GPS to Iridium satellite phone modules, the RPDA-57 continues to deliver mission-specific value. Currently over fifteen thousand Elbit RPDAs are deployed for use by the United States Army and the United States Marine Corps, in addition to several international military forces. The RPDA is used in a variety of applications from inventory management, vehicle maintenance, target designation, medical triage and Blue Force Tracking.

Elbit Systems of America, Fort Worth, TX. (817) 234-6799. [www.elbitsystemsofamerica.com].

Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected

Digital Compass Is Compact and Tilt Compensated

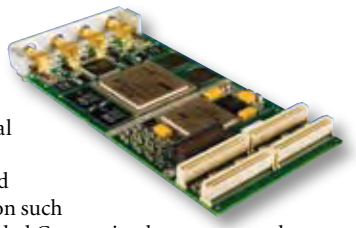


Once an exotic idea, embedded digital compass technology has become a pervasive requirement in a variety of military systems. A new family of highly accurate, 3-Axis solid-state OEM digital compasses that measure 1-inch square and offer a wide range of connection options is being introduced by OceanServer Technology. OS5000 Digital Compasses incorporate 3-Axis magnetic sensors with 3-Axis accelerometers to provide 0.5 degrees nominal accuracy, 0.1 resolution, ±180 degree roll, ±90 degree tilt, and include electronically gimbaled tilt compensation. Suitable for a variety of OEM applications, they measure only 1 inch square x 0.3 in., weigh less than 2g and can be connected via RS-232, TTL, or USB.

Featuring an ASCII interface, hard- and soft-iron calibration and user-configurable data formatting, OS5000 Digital Compasses provide up to 40 Hz data update rate. Standard features include a 50 Mips processor supporting IEEE floating-point math, a 24-bit A-D converter, programmable baud rate from 4,800 to 115,000 baud, and less than 20 mA at 3.3V power consumption. OS5000 Digital Compasses are priced at $249 each or $199 each for 10, with larger quantity discounts offered.

OceanServer Technology, Fall River, MA.
(508) 678-0550. [www.ocean-server.com].

Dual-Channel 16-Bit Digital Receiver Rides XMC



Demanding signal acquisition applications—such as radar, software defined radio (SDR), and signal intelligence (SIGINT) platforms—have a heavy appetite for modular high-speed digital receiver technology. Delivering on such needs, Curtiss-Wright Controls Embedded Computing has announced the availability of the XMC-E2201, a rugged and compact high-speed, dual-channel 16-bit digital receiver XMC/PMC mezzanine card. The XMC-E2201 supports analog sampling rates of 160 Msps and speeds the integration of high-performance signal acquisition into rugged deployed COTS VPX, VME and CompactPCI subsystems.

Based on twin Xilinx Virtex-5 FPGAs, the XMC-E2201 combines input bandwidth in excess of 700 MHz, industry-leading signal-to-noise ratio rated at greater than 77 db, and high spectral purity. This small form factor mezzanine card delivers high dynamic range for sophisticated digital signal processing. Its twin FPGA architecture dedicates one "DSP" Virtex-5 FPGA for high-speed acquisition of the dual analog channel inputs. An eight-lane PCI Express (PCIe) interconnect provides direct high-speed off-board data throughput rates up to 2.5 Gbytes/s. The XMC-E2201 is designed to operate in rugged environments and is available in a range of air- and conduction-cooled formats. Pricing for the XMC-E2201 starts at $9,620. Availability is Q2 '08.

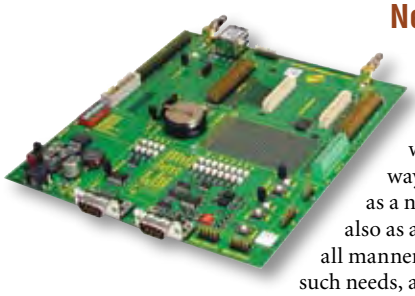
Curtiss-Wright Controls Embedded Computing, Leesburg, VA.
(703) 779-7800. [www.cwcembedded.com].

Thermal Controllers Are Military Approved

Reliable thermal control ranks as a critical design issue for a variety of in-theatre military systems. Serving that need, Degree Controls has announced a new line of Military-approved thermal controllers for electronics applications. Ruggedized for high-reliability, mission-critical Military applications, the new line of fully configurable, standard controllers offers Military contract manufacturers increased reliability and reduced time-to-market. DegreeC's CAGE Code is 45R61, and the company is ITAR registered.

DegreeC's standard Military controller line is designed to meet both Mil-STD-461 (EMI/EMC) and Mil-STD 810F (Environmental/Physical) testing requirements. These intelligent and ruggedized fan controllers leverage the company's proprietary software allowing for programmable alarm thresholds and fan curves. The onboard microcontroller controls or monitors fan speeds, communicates with the host through serial interfaces, measures temperatures, detects filter blockages and reports alarms. In addition to their thermal control products offering, DegreeC offers a full line of airflow sensors, switches and instrumentation devices appropriate for use in Military products. The company also features robust test and analysis services for Military electronics devices, including HASS, HALT, ESS, MTBF, MIL-STD-1629, MIL-HBK-217F, EMC/I and safety testing.

Degree Controls, Milford, NH. (603) 672-8900. [www.degreec.com].



Networking Module Tunes for App-Specific Interfaces

The military has warmed to Ethernet in a big way. It's being used not just as a networking technology but also as an interconnect scheme for all manner of data interfaces. Serving such needs, a new Ethernet networking module enables users to custom configure it for the specific needs of an application. The ConnectCore 9p 9215 from Digi International features two flexible interface modules (FIMs) built into the ARM9 microprocessor that will allow customers to load and use application-specific interfaces such as Secure Digital, Controller Area Network (CAN), 1-Wire, additional UARTs and others. Adding interfaces in the FIMs reduces complexity and overall product cost by minimizing the number of components necessary for a design. It also features advanced networking protocols like IPv6, SNMPv3 and SSL, which allows customers to easily upgrade protocols over time without having to replace hardware.

The ConnectCore 9P 9215 also offers an on-chip AES encryption engine that provides 10 times the secure data throughput of comparable software-based solutions. Digi JumpStart Kit development solutions are available. The ConnectCore 9P 9215 module is priced at $59 in quantities of 1,000. The JumpStart Kit is available for an introductory price of $399.

Digi International, Minnetonka, MN.
(952) 912-3444. [www.digi.com].

Dual-Head Graphics XMC Blends with Low Power

Avionics and military applications such as terrain overlay systems, graphic consoles and systems that render several live video channels—all these have something in common: they're all pushing the envelope of graphics requirements. Feeding such needs, a second-generation dual-head graphics XMC mezzanine card, the XMC-G72 from Thales Computers, fits any x8 PCI Express XMC-compliant SBC. The XMC-G72 incorporates 128 Mbytes on-chip GDDR3 memory and low power dissipation using the M72-CSP128 graphics controller from AMD/ATI technology. The M72-CSP128 graphics controller supports 2D and 3D acceleration as well as DirectX and OpenGL. The XMC-G72 mezzanine card features dual independent displays through two front connectors. Both digital DVI and CRT or dual CRT are offered. The rugged conduction-cooled build version of the XMC-G72 routes the digital DVI video output to the Pn4 rear I/O connector of the mezzanine.

The XMC-G72 interfaces with the single board computer using an x8 PCI Express link that peaks at 2.5 Gbytes/s, about ten times faster than graphics PMC mezzanine products currently available. This high throughput interface between the host CPU and the graphics controller significantly improves the performance of applications that intensively use bitmap transfers. Samples of the commercial build version of the XMC-G72 are currently available. The rugged conduction-cooled version will be available in the second quarter of 2008.

Thales Computers, Edison, NJ. (732) 494-1010.
[www.thalescomputers.com].

Gbit Clustering Switch Enables Flexible Net Management

IP-based packet networking has become entrenched as the vision for future DoD networking. A new Gbit switch from SMC Networks employs a single chip architecture to ensure wire-speed delivery of data packets while maintaining security through the use of SSL, SSH and other security measures required by today's networks. The TigerSwitch 10/100/1000 from SMC Networks provides flexibility in network configuration. It incorporates power over Ethernet (PoE) and an IP clustering solution that facilitates grouping switches for efficiency and network extension with other SMC81-Series Gigabit Switches or SMC61-Series Fast Ethernet Switches. Its support for PoE makes placement of network components and accessories like IP phones and cameras that require power, easy and flexible.

The 8124PL2 is the newest in SMC's TigerSwitch family of edge switches, which includes the 50-port 8150L2 and 26-port 8126L2. All three are designed to provide a flexible, extensible management architecture for growing and changing networks—from the SMB to the Enterprise. And, flexibility goes beyond PoE and clustering—the SMC8124PL2 has two combo ports that accept 1000BASE-SX, -LX or -ZX mini GBIC transceivers. The 24-port SMC8124PL2 is priced at $1,199.99.

SMC Networks. Irvine, CA. (800) 762-4968. [www.smc.com].

Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected

Simulink-Based I/O "Cube" Offers Flexible I/O

An entire community of system developers has rallied around The MathWork's Simulink tool, and military system developers are well represented among them. Models built in The Mathworks' Simulink can now be deployed directly on a new and flexible I/O target called UEISIM from United Electronic Industries (UEI). Once programmed using The Mathworks' Real-Time Workshop, the UEISIM can operate stand-alone, or may be continuously monitored by a host computer over the Cube's Ethernet port. This offers the Simulink user a new tool for the creation and tuning of a wide variety of defense applications, including simulation model verification, rapid prototyping and hardware-in-the-loop testing.

The UEISIM 300 allows the installation of up to 3 I/O boards. The UEISIM 600 is slightly larger at 4x 4.1x 5.8-inches and allows the installation of up to 6 I/O boards (containing up to 150 analog inputs or 288 DIO). The I/O boards installed are determined by the user's application. There are currently over 30 different I/O boards available including analog input, analog output, digital I/O, counter/Timer, quadrature Encoder, serial I/O, CAN bus and ARINC-429 interfaces. Pricing for the UEISIM 300 is $1,995 and $12,295 for the UEISIM 600.

United Electronic Industries, Walpole, MA.
(508) 921-4600. [www.ueidaq.com].

Dual-Bridge Motor Driver Has Selectable Overcurrents

The name of the game for military motor control systems is the blend of low power and high performance. Along just those lines, the 7I29 from Mesa Electronics is a Dual H bridge driver for two brush-type motors or other inductive loads. The 7I29 is rated at 15A continuous at 175 VDC per axis. Each bridge on the 7I29 has selectable overcurrent limits of .75 times and 1.5 times rated current. Low on resistance MOSFETs and high-performance gate drivers give the 7I29 high efficiency and low dead time to support switching rates up to 100 KHz. Gate power is derived from logic side power so that unlike other bridges, the drivers are functional all the way down to 0V motor power supply, allowing safe and easy initial setup and testing.

The 7I29 has 2500V RMS isolation from motor power to logic side control signals. The 7I29 also includes encoder input conditioning. Encoder inputs can be either single-ended or differential. The 7I29 is compatible with Mesa's 4I27 or the 4I34M, 4I65, 4I68, 5I20, 5I22 and 7I60 Anything I/O cards with SoftDMC or HostMot firmware, or can be used with a customer-supplied controller. Price of the 7I29 is $205 in 100s.

Mesa Electronics, Richmond, CA.
(510) 223-9272. [www.mesanet.com].

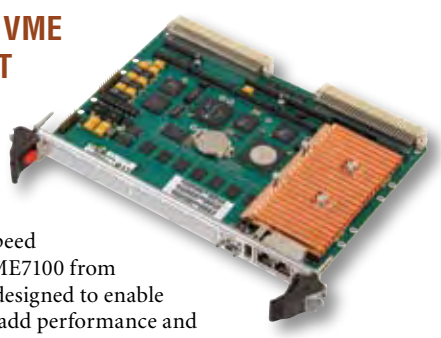
ATX Boards Sport Core2 Duo, Quad CPUs

Obsolescence presents a serious problem for military system designers. And the problem isn't going away any time soon. Two new ATX motherboards support Intel Core2 Duo and Quad processors are designed specifically for embedded applications requiring a stable revision-controlled platform, with long-term availability. Using the Intel Q35 Express chipset, the boards introduced by Itox have guaranteed availability through December 2012. The LGA775 socket supports a wide range of Intel Embedded Architecture processors, including the Intel Core2 Quad processors, Intel Core2 Duo processors and Intel Celeron 400 series processors with 800, 1067 and1333 MHz front-side bus speeds.

The Itox model BL630-DR motherboard utilizes an Intel ICH9DO Southbridge providing RAID 0, 1, 5 and 10 disk configuration using Intel Matrix Storage Technology. Optimized for the Intel Core2 Quad processor, the BL630-D and BL630-DR motherboards retain full compatibility with Intel Core2 Duo processors and Intel Celeron 4xx sequence processors. Maximum performance is leveraged with up to 8 Gbytes of DDR2 800 MHz dual-channel memory, dual PCI Express Gbit Ethernet controllers and onboard Intel GMA 300 graphics accelerator. Pricing for the BL630-DR is $400 and for the BL630-D $390 with volume pricing available.

Itox, East Brunswick, NJ. (732) 390-2815. [www.itox.com].

Dual-Core PowerPC VME Board Runs at 2eSST Rates



The era of dual-core processors is rolling into full swing. Featuring a dual-core PowerPC processor and 2eSST high-speed VMEbus interface, the MVME7100 from Emerson Network Power is designed to enable defense/aerospace OEMs to add performance and features for competitive advantage while providing backward compatibility to protect their investment in VMEbus technologies. The MVME7100 offers flexibility to support varying I/O requirements with the same base platform, simplifying part number maintenance, technical expertise requirements and sparing. It also provides optimal speed, which is achieved due to the independence of the PCI buses for each PMC site. In addition, the board's non-volatile memory feature prevents system memory loss in the event of a power loss.

The MVME7100 is based on the system-on-chip Freescale MPC8641D with dual PowerPC e600 processor cores, high-capacity DDR2 memory, up to 8 Gbytes of NAND Flash, PCI-X, USB and 2eSST. The MVME7100 series features dual integrated memory controllers, DMA engine, PCI Express interface, Gbit Ethernet and local I/O. The system-on-a-chip implementation offers power/thermal reliability and lifecycle advantages not typically found in alternative architectures. The MVME7100 also supports packages for VxWorks and Linux. The MVME7100 will be available in July 2008 with prices starting at $5,495.

Emerson Network Power, Tempe, AZ. (800) 759-1107. [wwwemersonnetworkpower.com].

COM Express Card Meets Intensive Graphics Needs

The Military's push toward Net-Centric Operations means they need power display interfaces at the nodes of that network. Designed for high-performance and graphic-intensive applications, a new COM Express CPU module from Arbor Solutions supports the Intel Core2 Duo processer and the 945GME/ICH7M chipset. The EmETXe-i9455 delivers integrated graphics performance with the Intel 945GME's Graphics Media Accelerator 950. The GMA 950 graphics core supports dual display, CRT and LVDS. Onboard DDRII SODIMM socket has a maximum memory capacity of 1 Gbyte. Additionally, EmETXe-i9455 is equipped with all required interfaces including PCIe x16 slot, three PCIe x1 slot, PCIe Gbit Ethernet, ATA, two SATA-II, two serial ports, eight USB 2.0 ports, KB/MS and AC97 Audio.

EmETXe-i9455 is RoHS-compliant and supports Advance Power Management (APM) 1.2 and Advanced Configuration and Power Interfaces (ACPI) 2.0 for optimized power management and system reliability. EmETXe-i9455 supports many mainstream operating systems, such as Windows 2000/CE/XP and Linux. It is fully compliant with the COM Express industry standard controlled by the PICMG.

Arbor Solution, San Jose, CA.
(408) 452-8900. [www.arborsolution.com].

Ethernet Switches Boast Slim Form Factor

The wide proliferation, longevity and bandwidth roadmap of Ethernet are just what long lifecycle designs in the military need. Aaxeon has released slim line models of its Lanolinx line of Industrial Ethernet Switches. In order to meet the demands for rugged Ethernet switches that minimize panel space requirements, the company's line of Unmanaged Ethernet Switches that are 45% thinner than its previous models. The current models being released have four 10/100 Copper ports and either one or two 100FX Fiber ports. Both single mode and multi-mode models are available.

The design of the LNX-501A and LNX-602A units offers an attractive price performance ratio. Unlike other products on the market that use plastic housings on their thinner models, Aaxeon maintains a metal housing with an IP-30 rating. In addition, they have maintained the industrial temperature ratings of -10° to 70°C. The units also have a Redundant Power Input and a Contact Closure for a local alarm. Prices for the LNX-501A and LNX-602A start at $169.

Aaxeon Technologies, Brea, CA.
(714) 671-9000. [www.aaxeon.com].

Advertisers Index

Get Connected with technology and companies providing solutions now

Get Connected is a new resource for further exploration into products, technologies and companies. Whether your goal is to research the latest datasheet from a company, speak directly with an Application Engineer, or jump to a company's technical page, the goal of Get Connected is to put you in touch with the right resource. Whichever level of service you require for whatever type of technology, Get Connected will help you connect with the companies and products you are searching for.

www.cotsjournalonline.com/getconnected

COTS Journal (ISSN#1526-4653) is published monthly at 905 Calle Amanecer, Suite 250, San Clemente, CA 92673. Periodicals Class postage paid at San Clemente and additional mailing offices. POSTMASTER: Send address changes to COTS Journal, 905 Calle Amanecer, Ste. 250, San Clemente, CA 92673.

Index

Coming Next Month

COTS JOURNAL

- *Stand-Alone Rugged Boxes* The New Trend in Defense. In the defense realm a trend has been building in the past couple years where traditional embedded board vendors are adding stand-alone rugged box-level systems to their military market offerings. These complete system boxes—which often support standard form-factor boards inside them—provide a complete, tested and enclosed computing solution that eliminates complex integration chores for customers. This section looks at this emerging product class and outlines the problems they solve.
- *Space-Qualified ICs and Systems*. Space-based semiconductors and board-level systems must be capable of withstanding everything from intense radiation due to high-energy atoms to bombardments from neutrons and other particles. Right-sizing the appropriate level of radiation hardening is somewhat of an art. Articles in this section explore the radiation concerns facing space designers and update readers on radiation-hardened boards, subsystems as well ASICs, FPGAs and power components designed for those applications.
- *Military Batteries and Power Conversion*. Gone are the days when they can be an afterthought in the system design process. Today the choice of power supplies, power converters and batteries can rank as a make or break decision in embedded military computer systems. With more and more computing stuffed into smaller spaces, power has direct implications on the size, cooling and mobility of a system. Articles in this section examine technology trends affecting military batteries, DC/DC converters, power supply module bricks and slot-card power supplies (VME, cPCI and others).
- *PC/104 and EPIC Boards*. PC/104 has become entrenched as a popular military form factor thanks to its compact size and inherent ruggedness. Sweetening the deal, a number of special enclosure techniques are used to outfit PC/104 for extremely harsh environments. This Tech Focus section updates readers on these trends, along with a look at the new PC/104 follow-on cousin: EPIC. Also provided is a product album of representative boards.


DIVE
INTO
TECHNOLOGY
COMING TO A CITY NEAR YOU
rtecc.com
Real-Time & Embedded
computing conference

COTS

Editorial

Jeff Child, Editor-in-Chief

...No Matter How Small

Small form factor embedded computers—both standard and non-standard varieties—have occupied a key role in military system designs for a couple decades now—and that importance will only rise as Moore's Law keeps working its magic. The "magic" of semiconductor integration has pushed the definition of "system" down to where complete computing engines now easily fit within the area of a cocktail napkin. Included are boards in form factors such as PC/104, EPIC, mini-ITX, StackableUSB, COM Express, MicroETXexpress along with a variety of small non-standard boards. This class of small SBCs solves problems for applications that are severely space- or weight-constrained or where in the past only a fully custom solution would fit the volume requirement. Example systems along those lines include small UAVs, robotics, mission-specific handheld systems, intelligent munitions and many others.

As an editor whose covered this area of technology for nearly 20 years now, my impression of this industry segment is that it's been—until very recently—holding its breath. Although vendors of the PC/104 board community have enjoyed robust business and growth over the years, extensions, follow-ons or spin-off specifications from the PC/104 mothership have been rare and slow to emerge. As the default consortium for small form factor specifications, the PC/104 Consortium has brought a couple predeveloped form factors under its wing including EPIC and EBX. The Consortium's current executive members are AMD, AMP, Digital-Logic, Fastwel, Kontron, Lippert, RTD Embedded Technologies, VIA and WinSystems.

Last fall a new consortium was formed—separate from the PC/104 Consortium—called the Small Form Factor Special Interest Group (SFF SIG), by founding members Octagon, Samtec, Tri-M, VIA and WinSystems. This non-profit industry group's purpose is to develop, promote and support small form factor board specifications and related technologies. Among the projects the group has in mind are specifications that feature PCI Express, USB 2.0, LPC Bus, and other bus and I/O interfaces. Formats include SBCs with expansion, computers-on-module (COMs) and stackables.

I'm reluctant to comment on the "turf war" over small form factor specifications that's been simmering because of the overlap between the PC/104 Consortium and the SFF-SIG—I have long relationships with companies in both camps, and the overlap between the two makes it a tricky needle to thread anyway. The SFF-SIG has gone on record saying it doesn't intend to compete with existing trade organizations, but rather to address new market needs and specifications that are not yet managed by a trade group. From my point of view "more is better" in this critical area of embedded technology. So if the two groups engender healthy competition, that will only benefit the military market.

Both groups stepped up their marketing efforts this month with some press events at the ESC Silicon Valley conference. ESC has always been the key marketing show for the PC/104 and small form factor board vendor community. ESC has also been the venue for the PC/104 Design Contest for which I've been on the judge's panel several times. This month at ESC, the PC/104 Consortium held a press event to promote its new PCI/104-Express and PCIe/104 specifications. PCI/104-Express provides a stackable PCI Express architecture while also providing a PCI bus. For additional room on a module, the PCIe/104 removes the PCI bus. The group intends for this new stackable PCI Express bus to be immediately incorporated across the Consortium's 104, EPIC and EBX form factors.

The Small Form Factor SIG meanwhile held a press dinner event at ESC where they discussed new technologies and platforms the group is working on. One of these was the adoption—announced earlier this month—of VIA's Pico-ITX specification to the SFF-SIG. The SFF-SIG is drafting a formal specification document and is promoting it with the goal of broadening the number of suppliers and customers who build and purchase Pico-ITX-compatible SBCs. The SIG intends to publish that specification within the next few months. Among the SFF-SIG's announcements at ESC this month was a form factor spec called Express104. It's defined as a stackable, 90mm x 96mm size board which employ's the SFF-SIG's SUMIT I/O scheme. SUMIT collects PCI Express, USB, SPI, I2C, and LPC Bus expansion into two, footprint-efficient, 52-pin, high-speed rugged Samtec Q2 connectors. Quite conveniently,---from a marketing point of view---it just so happens that 52 plus 52 equals 104, hence the name Express104. It's good to see the small form factor board vendors as a whole stepping up their marketing and technology development efforts.

If you'll indulge me, I'll even describe the new landscape as "Dr. Seuss-like" in terms of the apparent new imagination and zeal in the industry to raise the bar. I was recently helping my daughter with a book report about Dr. Seuss, so I've got him on the brain at the moment. The exaggerated illustrations, poetic meters and clever turns of phrase in Dr. Seuss books truly stretch the imagination beyond the typical children's book. As an adult, that famous line from Dr. Seuss's Horton Hears a Who! "A person is a person, no matter how small," and what it says about the evils of oppression and discrimination, gives me chills. And speaking of PC/104, if Dr. Seuss (Theodor Seuss Geisel) were alive today, he would have turned 104 years old last month. I'm going to call that a good omen looking forward to this year's developments in PC/104 and in other form factors…no matter how small. ▮▮

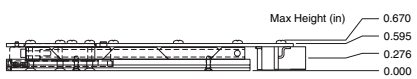
Loading this small size, light weight, power dense unit in your systems allows more room for the real power

Aegis VME450, reliable, rugged and ready to take care of business

The single-slot VME450 power supply — filtered 28 Vdc, four output (3.3, 5, ±12 V), 550 W — is a military COTS solution that is compliant to the vibration requirements of MIL-STD-810F and EMI per MIL-STD-461E. When compared to VME power supplies using conventional technology, the one-slot VME450 provides users with higher efficiency (85%), lower weight (2.4 pounds), and higher power (up to 550 W). Built with Vicor V•I Chips, it uses two M-FIAM modules, six PRMs and six VTMs.

Features

- Vin max range: 18 to 36 Vdc
- Temperature: –40 to +85˚C
- Output power: 550 W
- Input power: 650 W
- 28 Vdc per MIL-STD-704F
- 4 Output voltages, 550 W
- Meets MIL-STD-461E conducted EMI
- Utilizes Vicor's V•I Chips
- Single slot VME
- High efficiency: 85%
- Lightweight: 2.4 lb.



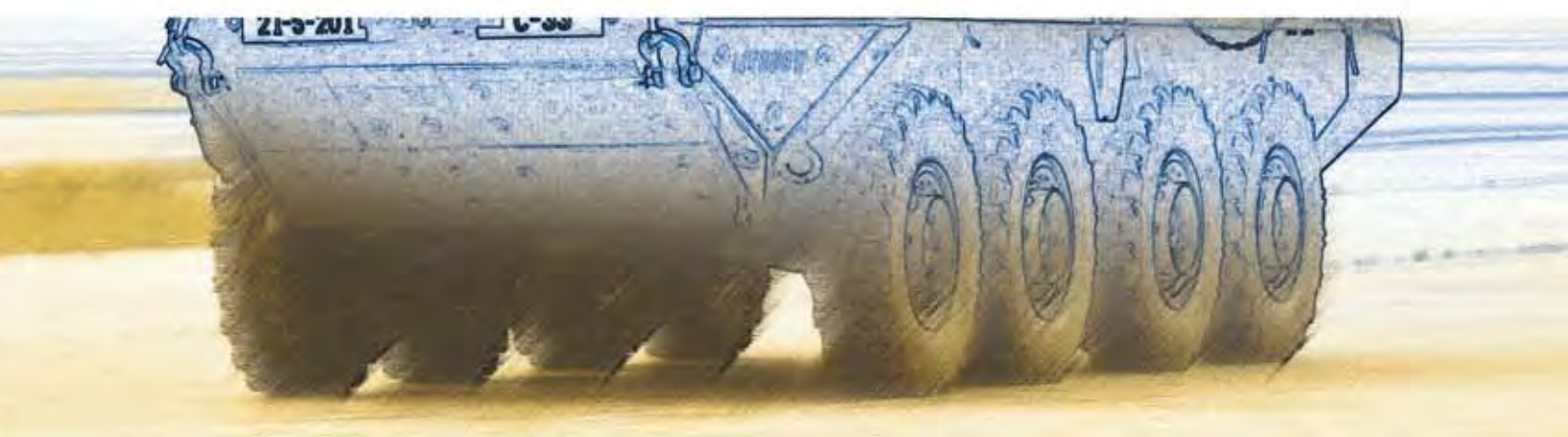
vicorpower.com/vmecj

Fill out your application details and qualify for a Vicor Pocket Reference Book or call 800-735-6200. Offer good while supplies last.

AEGIS Power Systems, Inc.

VICOR INTEGRATION ARCHITECT

Vicor *1.800.735.6200 • vicorpower.com*

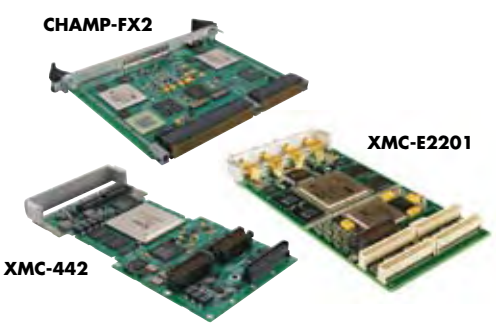


TOUGH DSP SOLUTIONS FOR TOUGH ENVIRONMENTS

Today's critical missions demand tough solutions. Solutions built to survive the harshest environments. Today's warfighters rely on rugged deployed sensor platforms with sophisticated signal and image processing for vital real-time information. Now, FPGA-based embedded computing takes sensor platform capabilities to a whole new level, delivering dense processing on low-power platforms.

Curtiss-Wright offers a range of rugged FPGA-based processing platforms. They include our full-featured VPX-based CHAMP-FX2 heterogenous processing module and the new compact XMC-E2201 signal acquisition mezzanine board. Each features comprehensive board support packages, software drivers, and advanced FPGA development kits to speed and ease application development and system integration.

If your system requires high performance sensor data processing, or your challenge is to reduce space, weight, and power consumption, Curtiss-Wright has the rugged, embedded FPGA platform for you. You work in a tough world. We thrive on the tough solutions.



Curtiss-Wright's FPGA processing boards for tough DSP, image processing, or signal acquisition include the CHAMP-FX2 and the XMC-442 FPGA processing modules, and the XMC-E2201 signal acquisition module.

CURTISS WRIGHT Controls
Embedded Computing

www.cwcembedded.com

RUGGED FPGA PROCESSING... *ABOVE & BEYOND*